KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
B.Sc. Engineering 2nd Year 1st Term Examination, 2023
Department of Computer Science and Engineering
CSE 2103
Microprocessors and Microcontrollers

TIME: 3 hours FULL MARKS: 210

N.B. i) Answer **ANY THREE** questions from each section in separate scripts.
ii) Figures in the immediate right column of the questions indicate full marks.
iii) The rightmost column indicates the course outcomes.

SECTION A

(Answer **ANY THREE** questions from this section in Script A)

1. a) What is addressing mode? Use `MOV` instruction to illustrate different types of addressing modes. (10) [CO4]
   b) What is pipelining in a microprocessor? (05) [CO1]
   c) Show the stack mapping of the following instructions. (08) [CO4]

```
DID PROC FAR
PUSHF
PUSH AX
PUSH BX
PUSH CX
.
.
.
POP CX
POP AX
POP BX
POPF
DID ENDP
```

   d) If a code segment starts at address `1210H`, then what will be the value of `IP` to point at the middle address of the code segment? What will be the value of the middle address? Consider the memory space as 16 MB, `CS` and `IP` have the same width. (12) [CO1]

2. a) Why 8086 is called a 16-bit microprocessor? What are the types of `JUMP` instruction in 8086? Describe them with examples. (10) [CO1]
   b) Demonstrate that `CMPSB` instruction can be used to compare two strings where they have (i) Equal length; and (ii) Different length. (10) [CO2]
   c) Write the machine codes for 8086 of the following instructions with detail rationale (template and others). (15) [CO3]
      i) `MOV BL, DH`
      ii) `MOV DX, [SI + 05H]`
      iii) `MOV BP, 04H[BX]`

3. a) Show that a stack can be used to pass parameters while converting `BCD 17H` to its corresponding binary number. (11) [CO1]
   b) How can you bypass the main processor while transferring data between memory and peripheral devices? Explain the process with necessary figure. (10) [CO2]
   c) Write the instructions to set or reset the trap flag. Explain in brief how these instructions perform in the desired function. (08) [CO4]
   d) If a microprocessor is defined as n-bit, then describe what is meant by n. (06) [CO1]

4. a) "`CMP` instruction is an application of subtraction operation" – justify the statement with necessary example. (10) [CO1]
   b) What do you mean by Cortex-M3? Describe its architecture with the necessary figure. (10) [CO2]
   c) Consider a processor with a clock speed of 10 MHz. Now, determine the value of `N` for the following program to generate an `X` μs delay. (`X` = last four digits of your roll no.) (15) [CO1]

```
MOV CX, N
Here: NOP
      NOP
      NOP
LOOP Here
```

SECTION B

(Answer **ANY THREE** questions from this section in Script B)

5. a) Why is a math coprocessor necessary? Explain the co-ordinated interaction between 8086 and 8087 in a system. (11) [CO2]

   b) Suppose the status register of 8087 holds '1000H' and the tag register contains '000FH'. Now, show the conditions of it's stack after performing the following operations sequentially. (12) [CO2]
      i) After 3 PUSH operations.
      ii) After 1 POP operation.

   c) Describe the operation of 8254 PIT with necessary diagrams after programming in the following way. (12) [CO4]
      i) A_1, A_0 = 11; CW = 14H; $\overline{WR}$=0; D_0 – D_7 = 02H
      ii) A_1, A_0 = 11; CW = C2H

6. a) Is it possible for the 8051 microcontroller, which has only 128 bytes of RAM built-in, to have more RAM? If so, how can the 8051 interface with the external RAM? (09) [CO3]

   b) Write the program to generate square wave and explain the associated timer mode using timer 0 of 8051 microcontroller. Assume the crystal oscillator of 8051 has a frequency of 12Hz. (12) [CO2]

   c) Design a traffic light system using 8051 μc. (14) [CO3]
      i) Provide necessary pin diagram.
      ii) Write the program in C language.

7. a) Given the arrival times and types of interrupts, analyze the sequence in which the 8051 μc will service these interrupts, considering the hexadecimal value '9DH' is loaded into the Interrupt Enable Register (IE) and '19H' is loaded into the Interrupt Priority Register (IP). (10) [CO3]

Arrival Time	Interrupt Type
1	INTO
2	RI + TI
3	TFO
3	INT1
3	TF1

   b) How the address space of 80286 microprocessor can be extended upto 1GByte, even though the width of its address bus is 24bit. Describe the technique with proper diagram(s). (12) [CO2]

   c) Tabulate the value of signals A_0, $\overline{BHE}$=0, memory banks, location accessed, D_0-D_7, D_8-D_{15}, for the following transfer operations. (13) [CO1]
      i) μp writes a byte 11H into location 1000:0003H.
      ii) μp writes a word 2211H into location 1000:0003H.
      iii) μp writes a byte 11H into location 1000:0004H.
      iv) μp writes a word 2211H into location 1000:0004H.

8. a) Despite the Intel 8085 having only 16 address lines, it is possible to expand its memory beyond 64 KBytes without resorting to virtualization. Describe this technique with appropriate illustrations. (11) [CO1]

   b) Explain the role of the descriptor tables in a 386 system with necessary sketches. (08) [CO2]

   c) The 80286 can't easily switch back and forth between real and protected addressing modes. Some argue that this limitation is actually a necessary feature. To what extent do you agree with this perspective? (08) [CO1]

   d) Memories starting at even address take 1 cycle, whereas those starting at odd address require 2 cycles. Explain this phenomenon by providing an example. (08) [CO3]

KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
B.Sc. Engineering 2nd Year 1st Term Examination, 2023
Department of Computer Science and Engineering
CSE 2105
Data Structures and Algorithms

TIME: 3 hours FULL MARKS: 210

N.B. i) Answer **ANY THREE** questions from each section in separate scripts.
ii) Figures in the immediate right column of the questions indicate full marks.
iii) The rightmost column indicates the course outcomes.

SECTION A

(Answer **ANY THREE** questions from this section in Script A)

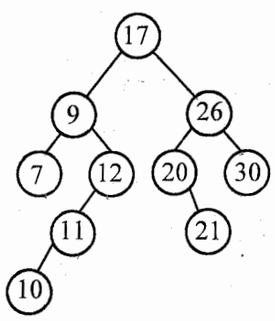
1. a) What is data structure? Distinguish between data structure and data type. (06) [CO1]
   b) How to calculate the element address in two-dimensional array. Consider the declaration of a 2D array is `A[8][16]`. The location of `A[0][0]` is 400. Where $w = 6$. (14) [CO1]
      i) Where is the location of `A[4][2]` if the row major representation is used?
      ii) Where is the location of `A[7][12]` if the column major representation is used?
   c) Write an algorithm modifying the binary search algorithm to insert an item into a sorted linear array. (08) [CO1]
   d) Explain the procedure of inserting and deleting an element from a linear array. (07) [CO1]

2. a) Discuss the trade-off of data structure operations between linear array and link list. (06) [CO1]
   b) Define Stack. "Stacks are used where processing of data must be postponed until other conditions are fulfilled" – draw your opinion about the statement. (10) [CO2]
   c) How does polish notation simplify the process of expression parsing and evaluation in programming language? Translate the infix notation `A+B*(C-D)/E+F*G-H` to its equivalent polish notation using stack. (10) [CO2]
   d) Let you are given a postfix arithmetic expression. Write an algorithm to evaluate the value of the given expression. (09) [CO2]

3. a) What is the purpose of the partition procedure in Quicksort? (05) [CO4]
   b) The pre-order and in-order of a tree T yield the following sequences of nodes. (10) [CO3]

Pre-order	1, 2, 4, 5, 7, 3, 6, 8
In-order	4, 2, 7, 5, 1, 8, 6, 3

   Draw the diagram of the tree T.
   c) What are the moves allowed by the solution of Towers of Hanoi problem when $n = 4$ disks? (10) [CO3]
   d) Consider the following binary search tree T. Show stepwise, the In-order traversal result of T after the key 17 is deleted. (10) [CO3]



4. a) Consider the following dequeue of characters where $DEQUE$ is a circular array which is allocated six memory cells: $LEFT = 2$, $RIGHT = 4$, $DEQUE$: _, A, C, D, _, _. Describe the dequeue while the following operations take place. (12) [CO2]
      i) F is added to the right of the dequeue.
      ii) Two letters on the right are deleted.
      iii) K, L, and M are added to the left.
      iv) One letter on the left is deleted.
   b) Suppose queue is stored in a circular array with $N = 10$ memory cells. (09) [CO2]
      i) Find the number of elements in a queue when $FRONT = 2, REAR = 6$.
      ii) When will the array be filled?

c) Construct a down-heap H from the following list of numbers: (14) [CO3]

20, 25, 35, 38, 50, 2, 55, 77, 82, 22

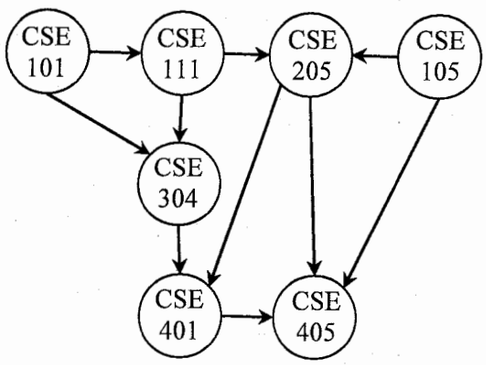
i) Insert another item 70 into constructed heap.
ii) Then delete the number 22 for replacing it.

SECTION B

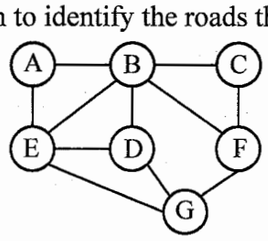
(Answer **ANY THREE** questions from this section in Script B)

5. a) Can a sorted linked list facilitate logarithmic time search for an element? If so, outline design for such a linked list; if not explain why it is not possible. (12) [CO1]
   b) If space complexity is not a limiting factor, which sorting algorithm would you prefer: quick sort, merge sort or radix sort? Provide a time complexity analysis to support your decision. (10) [CO4]
   c) Suppose you have two arrays both of size N, and you need to determine if they contain the same set of numbers. Provide a solution that works in linear time and requires constant space. Is this solution guaranteed to provide correct answer always? Give a brief explanation. (13) [CO4]

6. a) What are the pros and cons of using a doubly linked list for implementing the separate chain method in collision resolution? (07) [CO1]
   b) How can radix sort be adopted to efficiently sort an array of floating-point numbers ranging from -1000 to 1000, with upto two decimal places? Provide a solution and evaluate its time and space complexity. (14) [CO4]
   c) Consider the following course dependency graph. An edge from course x to course y indicates that course x must be completed before course y can be taken. Design an algorithm to find a sequential order of courses that a student can undertake. Also find a sequence for the given graph applying your proposed algorithm. (14) [CO3]



7. a) Which sorting algorithm would you prefer to sort a linked list? Explain with proper complexity analysis. (08) [CO1]
   b) Design an algorithm that will find the index of the first and last occurrence of a target value in a sorted array of size N. The time complexity of your proposed algorithm should not exceed $logN$. (12) [CO4]
   c) Consider the following graph. Here each node represents a city and each edge represents a road that can be build to connect two cities. Your goal is to minimize road construction costs by removing redundant roads ensuring every city remains reachable from any other city. Develop an algorithm to identify the roads that can be eliminated. (15) [CO3]



8. a) You are building a web browser. You want to integrate the backward and forward navigation functionality using a doubly linked list, all the while ensuring minimal memory usage. Define the node structure and devise functions for both backward and forward navigation. Assume each web page is represented by an integer value. (12) [CO1]
   b) Do the chosen graph representation methods affect the complexity of graph traversal algorithms? Explain with a detailed complexity analysis. (08) [CO3]
   c) Which data structure would you prefer when the task involves repeated searching for a specific value and inserting elements in random order: an array or a heap? Justify your answer. (08) [CO1]
   d) Is it possible to find the shortest path between two nodes using BFS when the graph is weighted? Explain with proper example. (07) [CO3]

KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
B.Sc. Engineering 2nd Year 1st Examination, 2023
Department of Computer Science and Engineering
MATH 2107
Fourier Analysis and Linear Algebra

TIME: 3 hours FULL MARKS: 210

N.B. i) Answer **ANY THREE** questions from each section in separate scripts.
ii) Figures in the immediate right column of the questions indicate full marks.
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SECTION A

(Answer **ANY THREE** questions from this section in Script A)

1. a) Define causal and non-causal system of equation with example. (05) [CO1]
   b) Test whether the following system of equations are causal or not. (09) [CO2]
      i) $y(t) = tx(t)$.
      ii) $y(t) = x^2(t)$.
      iii) $y(n) = x(n) - x(n-1)$.
   c) Determine the z-transform of the signal $x(n) = [3(2^n) - 4(3^n)].u(n)$ and plot the Region of Convergence (ROC). (11) [CO2]
   d) Find $x(n)$ by using convolution property for $X(z) = \frac{1}{(1-\frac{1}{2}z^{-1})(1+\frac{1}{4}z^{-1})}$. (10) [CO2]

2. a) Write down the important properties of the ROC for z-transform. (09) [CO1]
   b) By applying the time shifting property find the signal of $X(z) = \frac{z^{-2}+\frac{1}{2}z^{-1}}{1-\frac{1}{2}z^{-1}}$. (06) [CO2]
   c) Find the inverse transform of $X(z) = \frac{z}{(z-1)(z-2)(z-3)}$ using partial fraction method in the ROC $2 < |z| < 3$. (11) [CO3]
   d) Find the Fourier cosine transform of $f(x) = \frac{1}{1+x^2}$ and hence derive the Fourier sine transform of $\varphi(x) = \frac{x}{1+x^2}$. (09) [CO3]

3. a) Write down the assumptions for the validity of Fourier series expansion. (07) [CO1]
   b) If $f(x + 2\pi) = f(x)$, find the Fourier series expansion of (14) [CO2]
   $f(x) = \begin{cases} -\pi, & -\pi < x < 0 \\ x, & 0 < x < \pi \end{cases}$.
   Hence prove that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \cdots = \frac{\pi^2}{8}$.
   c) Apply Parseval's identity to the function $f(x) = \sin x, 0 < x < \pi$ and show that (14) [CO3]
   $\frac{1}{1^2.3^2} + \frac{1}{3^2.5^2} + \frac{1}{5^2.7^2} + \cdots = \frac{\pi^2-8}{16}$.

4. a) Define integral transform and hence find the kernel of Fourier transform. (08) [CO1]
   b) Define odd and even functions. (04) [CO1]
   c) If $f(t) = t^2,\ 0 < t < 1$ find its half range Fourier sine series. (11) [CO2]
   d) Express the function $f(x) = \begin{cases} 1 & for\ |x| \le 1 \\ 0 & for\ |x| > 1 \end{cases}$ as a Fourier integral. Hence evaluate, (12) [CO3]
   $\int_0^\infty \frac{\sin\lambda \cos\lambda x}{\lambda} d\lambda$.

SECTION B

(Answer **ANY THREE** questions from this section in Script B)

5. a) Define with example (i) diagonal matrix, (ii) unit matrix, (iii) skew-symmetric matrix, (iv) upper triangular matrix. (12) [CO1]
   b) If $A = \begin{bmatrix} 2 & 1 & 0 \\ 3 & 2 & 0 \\ 1 & 0 & 1 \end{bmatrix}$ and $B = \begin{bmatrix} 1 & 1 & 1 & 0 \\ 2 & 1 & 1 & 0 \\ 2 & 3 & 1 & 2 \end{bmatrix}$ then find AB by partitioning. (08) [CO2]

c) Apply elementary transformations to find the inverse of the following matrix. (15) [CO3]

$$A = \begin{bmatrix} 1 & -3 & 2 \\ -3 & 3 & -1 \\ 2 & -1 & 0 \end{bmatrix}.$$

6. a) Define rank of a matrix. (04) [CO1]

b) Reduce the matrix A to its echelon form then to its canonical form then to its normal form. Also find its rank where, (14) [CO2]

$$A = \begin{bmatrix} 2 & 7 & 3 & 5 \\ 1 & 2 & 3 & 4 \\ 3 & 8 & 1 & -2 \\ 4 & 1 & 1 & -1 \end{bmatrix}.$$

c) Express the matrix $A = \begin{bmatrix} 2 & 1 & 3 \\ 1 & -1 & 2 \\ 1 & 2 & 1 \end{bmatrix}$ as the sum of a symmetric and skew-symmetric matrix. (06) [CO2]

d) Find the values of a for which the system has no solutions, exactly one solution, or infinitely many solutions. (11) [CO2]

$$x + 2y + z = 2$$
$$2x - 2y + 3z = 1$$
$$x + 2y - (a^2 - 3)z = a$$

7. a) Let X_z and X_w be the co-ordinates of a matrix with respect to given pair of basis. Determine the matrix P such that $X_w = PX_z$, where, $z_1 = [1, 0, 0]'$, $z_2 = [1, 0, 1]', z_3 = [1, 1, 1]'$ and $w_1 = [0, 1, 0]', w_2 = [1, 1, 3]', w_3 = [1, -1, 1]'$. (11) [CO3]

b) Define vector space and basis of vector space. (04) [CO1]

c) Show that the 4-vectors $v_1 = [2, 2, 2, 0], v_2 = [6, 5, 3, -2], v_3 = [3, 2, 0, -2]$ and $v_4 = [6, 4, 0, -4]$ over F span a vector space $v_4 2(F)$ and obtain the basis of the vector space. (10) [CO3]

d) Examine the following vectors for linear dependence and find the relationship if it exists. (10) [CO3]

$$x_1 = (1, 2, 4),\ x_2 = (2, -1, 3),\ x_3 = (0, 1, 2),\ x_4 = (-3, 7, 2)$$

8. a) Define inner product space with example. (08) [CO1]

b) Find all eigenvalues and bases for the eigenspace of the matrix $\begin{bmatrix} 4 & 0 & 1 \\ -2 & 1 & 0 \\ -2 & 0 & 1 \end{bmatrix}$. (15) [CO2]

c) Let, $\mathbb{R}^4$ have the Euclidian inner product. Apply the Gram-Schmidt process to transform the basis $\{u_1, u_2, u_3, u_4\}$ into an orthonormal basis, where $u_1 = (0, 2, 1, 0)$, $u_2 = (1, -1, 0, 0),\ u_3 = (1, 2, 0, -1),\ u_4 = (1, 0, 0, 1)$. (12) [CO3]

KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
B.Sc. Engineering 2nd Year 1st Term Examination, 2023
Department of Computer Science and Engineering
CSE 2113
Computer Architecture

TIME: 3 hours FULL MARKS: 210

N.B. i) Answer **ANY THREE** questions from each section in separate scripts.
ii) Figures in the immediate right column of the questions indicate full marks.
iii) The rightmost column indicates course outcomes.

SECTION A

(Answer **ANY THREE** questions from this section in Script A)

1. a) Why do you study computer organization and architecture? List the bottlenecks of Von Neuman architecture. (07) [CO1]
   b) In a computer system, main memory and cache memory ratio is 64: 8 and 16 bits are for addressing. Find TAG, BLOCK and WORD bits in (i) direct mapping when block size is 8 words, (ii) associative mapping when block size is 16 words, (iii) TAG, SET and WORD bits for set associative mapping for 4 blocks per set and 16 words per block. (15) [CO2]
   c) Explain the operating principle of static and dynamic RAM with appropriate figures. Which one is more energy efficient and why? (13) [CO2]

2. a) Describe the reasoning behind using the three-level memory organization. (10) [CO1]
   b) Describe the issues of SSDs caused by the fundamental limitations of NAND flash memory. Discuss about the renowned solutions to these issues. (10) [CO2]
   c) Choose the best replacement algorithms for the three main memory to cache memory mapping techniques. Justify your pick. (15) [CO2]

3. a) Define bus in terms of a computer system and state how many buses a computer may have, "If there is a data bus for data, shouldn't there be an instruction bus also?" –do you agree with this? Justify your opinion. (10) [CO1]
   b) Explain the reasoning behind the usage of two different kinds of RAM cells in computer organization. (10) [CO2]
   c) Calculate the check bits of Hamming error correcting code and show their layout (i.e., their relative positions around each other) for a given data $D = 10110001$. (15) [CO2]

4. a) What kind of disk layout method will you choose if you need to prioritize speed over storage efficiency? Justify your pick. (10) [CO2]
   b) Analyze three device identification techniques needed to design interrupt driven I/O. (15) [CO2]
   c) What are interrupts in a computer system? Describe the ways of handling multiple interrupts. (10) [CO1]

SECTION B

(Answer **ANY THREE** questions from this section in Script B)

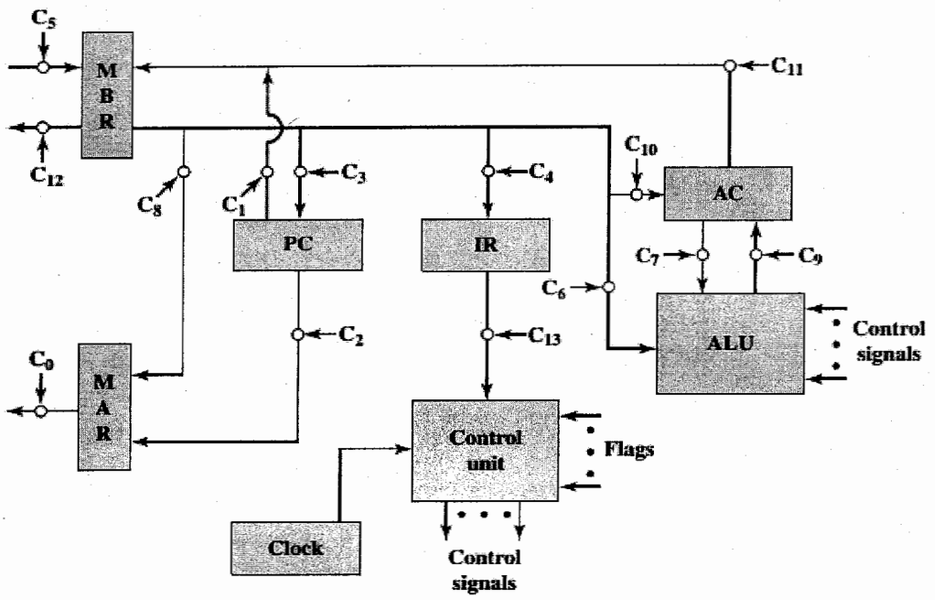
5. a) You are given a computer with following format for floating point representation: 1 sign bit, 6 exponent bit(s) and 4 significant bits. However, for a given problem, you require higher precision values without increasing bit numbers. Write down your solution for this problem and its impact on the system. (10) [CO1]
   b) Multiply $(-13)_{10}$ by $(5)_{10}$ using Booth's algorithm. Illustrate the reason behind requiring less operation for this algorithm with example. (15) [CO3]
   c) Define Guard bits. Write down the steps for performing floating point subtraction for the given two numbers with and without Guard bits and compare the results: 1.0000×2^1 and 1.1111×2^0 (there are 4 bits in significant field and ALU registers are 6 bits long). (10) [CO3]

6. a) Illustrate the branch history table approach with necessary explanation and diagrams. (12) [CO3]
   b) For a computer, the given table represents the different cycle times for pipeline stages: (10) [CO3]

Stage	IF	ID	FO	EI	WO
Delay	3ms	2ms	5ms	2ms	4ms

   i) What would be the speedup factor for the instruction pipeline compared without pipeline execution for a program with 10 instructions?
   ii) In some cases, pipeline results in greater latch delay. If we consider the delay to be 5ms, what would be the speedup factor for the same program execution?

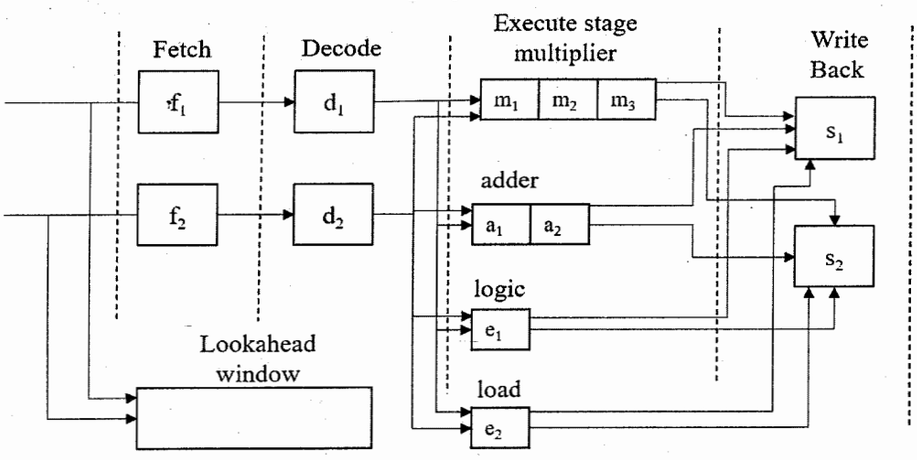
c) The following figure represents data and control paths of a computer. Write down the micro-operations, timing and control signals for the below instructions (for all stages): (i) `Load AC, (R1)`, (ii) `Store AC, M`, (iii) `BEQ AC, R1, Label # BEQ means branch if equal.` (13)



7. a) Explain the key characteristics of RISC architecture. (12) [CO3]
   b) Differentiate between superscalar and super pipeline approaches. For performing a division operation, which would be more suitable? Justify your answer. (08) [CO3]
   c) Consider the following program to execute in the processor. (15) [CO3]

Instruction Num	Instruction
I1	`Load R1, A`
I2	`ADD R2, R1, R8`
I3	`ADD R3, R3, R5`
I4	`MUL R3, R4, R5`
I5	`AND R6, R6, R7`
I6	`OR R2, R2, R5`

program



processor

   i) Identify the existing dependencies in the program.
   ii) Show the pipeline activity for this program with out-of-order issue with out-of-order completion (`I1` and `I4` require 2 cycles to execute and the lookahead window size us 16 instructions).

8. a) Explain the pipelining hazard scenario with proper example. (10) [CO3]
   b) Discuss about the instruction set design issues. (10) [CO3]
   c) Show the division operation for $(-12)_{10}$ by $(5)_{10}$ in ALU. Do the registers hold the same value for $(12)_{10}$ by $(-5)_{10}$? (15) [CO3]

KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
B.Sc. Engineering 2nd Year 1st Term Examination, 2023
Department of Computer Science and Engineering
EEE 2117
Analog Electronics

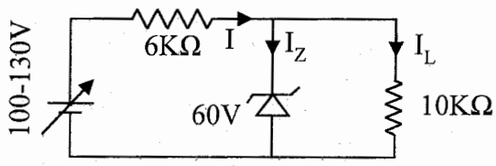
TIME: 3 hours FULL MARKS: 210

N.B. i) Answer **ANY THREE** questions from each section in separate scripts.
ii) Figures in the immediate right column of the questions indicate full marks.
iii) The rightmost column indicates course outcomes.

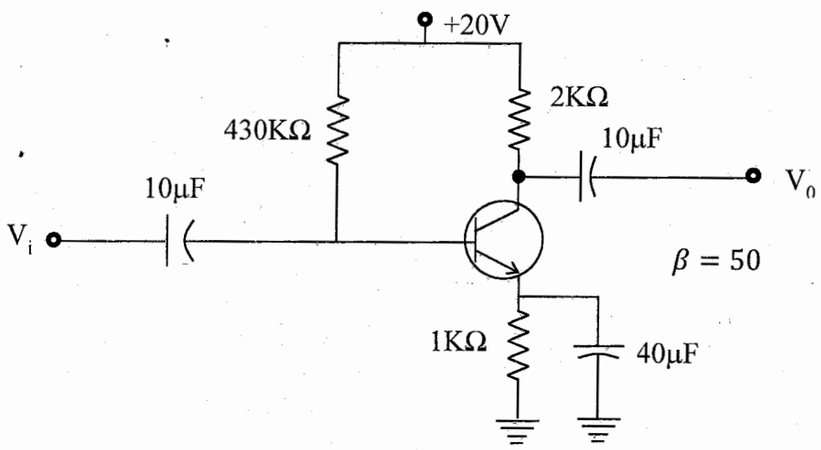
SECTION A

(Answer **ANY THREE** questions from this section in Script A)

1. a) Classify solids based on band diagram. Explain the formation process of potential barrier in a p-n junction (12) [CO1]
   b) Briefly explain the working principle of full wave bridge rectifier circuit. Show that the rectifier efficiency of full wave is twice to half wave rectifier. (13) [CO1]
   c) Draw the I-V characteristics of Zener diode. For the circuit shown in following figure, find the maximum and minimum values of Zener diode current. (10) [CO2]



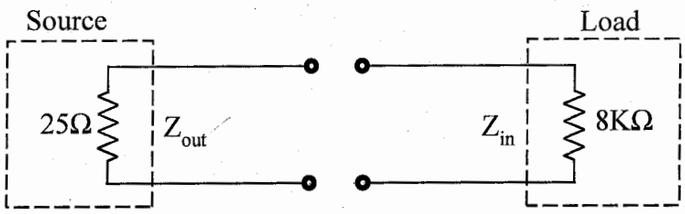
2. a) Define faithful amplification and stabilization. Explain the needs for stabilization. Prove that the stability factor, $S = \frac{\beta+1}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$; where the symbols have their usual meanings. (12) [CO1]
   b) Your employer asked you to design a transistor with proper power rating and provide the specifications below: (10) [CO1]
   (i) Maximum power rating $100mW$, (ii) $V_{CE} = 20V$, and $I_C = 5mA$.
   What would be your response?
   c) What are the essentials of a transistor biasing circuit? For the emitter-stabilized bias circuit in following figure, determine: (i) I_B, (ii) I_c, (iii) V_{CE}, (iv) V_C, (v) V_{BC}. Mention the application of Darlington pair circuit. (13) [CO1]



3. a) What are the types of filter circuits? Describe the operation of a capacitor input filter/π filter. (12) [CO4]
   b) What are the models used in small-signal *ac* analysis of transistor networks? Show that the voltage gain and current gain of a common emitter amplifier are: $A_v = -\frac{R_L}{r_e}$, and $A_I = \beta$, where the symbols have their usual meanings. Assume, $r_0 = \infty\Omega$. (12) [CO3]
   c) Graphically represent the depletion and enhancement mode of *n*-channel MOSFET. Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10mA$ and $V_P = -4V$. (11) [CO1]

4. a) Why a 'MOSFET' is named so? Describe the channel formation process in *n*-channel Enhancement-type MOSFET. (10) [CO1]
   b) Prove that $I_C = (\beta^2 + 2\beta)I_B$ for a Darlington pair transistor connection. (10) [CO2]

c) Your manager is concerned that if the source is directly connected to the load, small source power will be transferred to the load due to impedance mismatch. They want you to redesign the circuit that can transfer maximum power to the load. You have the option of choosing common base, common collector and common emitter connection. (08) [CO1]



d) Draw the schematic diagram of a *dc* power supply using a full wave bridge rectifier, *Rc* filter, and *Ic* regulator to provide an output $+12V$. (07) [CO2]

SECTION B

(Answer **ANY THREE** questions from this section in Script B)

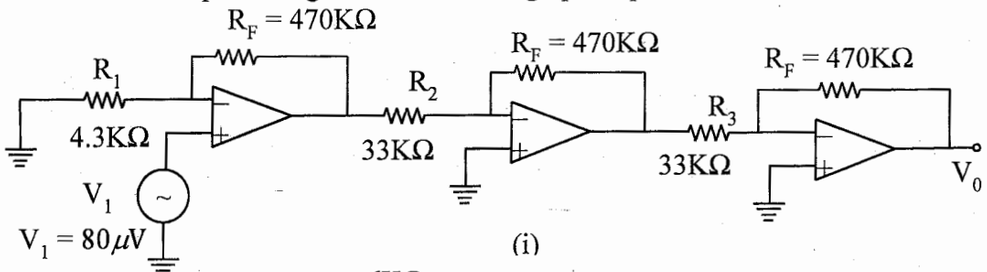
5. a) Explain the operation of UJT as relaxation oscillator and derive the expression for the frequency of generated saw-tooth wave from the oscillator. Why UJT is named so? (13) [CO1]
   b) Draw the two-transistor model of SCR. Explain V-I characteristics curve indicating all significant points. (10) [CO1]
   c) An SCR half-wave rectifier circuit is adjusted to have a gate current of $1mA$. The forward breakdown voltage of SCR is $150V$ for $I_G = 1mA$. If a sinusoidal voltage of $400V$ peak is applied, find: (i) firing angle, (ii) conduction angle, (iii) average output voltage, (iv) average output current for a load resistance of 200Ω, (v) power output, (vi) comment on the changes in average output current if firing angle is made larger. (12) [CO1]

6. a) What is the main advantage of TRIAC compared to SCR? Explain the 4 modes of operation of TRIAC with relevant diagram and indicate these modes in the *V-I* characteristics curve of TRIAC. (10) [CO1]
   b) Power of a $100W, 110V$ tungsten lamp is to be varied by controlling the firing angle of an SCR in a half-wave rectifier circuit supplied with $110V$ *ac* (*rms*). What *rms* voltage and current are developed in the lamp at firing angle $\alpha = 60°$? (12) [CO1]
   c) What are the differences between DIAC and TRIAC? Explain the operation of a heat control circuit consisting of DIAC and TRIAC with necessary diagram. (13) [CO1]

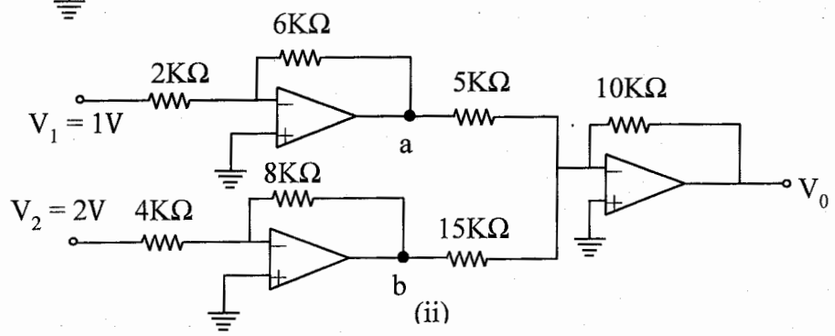
7. a) Define op-Amp. Derive the equations of output voltage of an op-Amp inverting and non-inverting amplifier from their respective *AC* equivalent circuits. (12) [CO4]
   b) Design op-Amp circuits that provide the following output voltages: (11) [CO4]

$$\text{(i) } V_0 = 4V_1 - 10\frac{dV_2}{dt}, \text{ (ii) } V_0 = 3\int V_1 dt + 12V_2.$$

   Assume V_1 and V_2 are two input voltages and V_0 is the output voltage.
   c) Calculate the output voltages of the following op-Amp circuits: (12) [CO4]



(i)



(ii)

8. a) Define and classify UPS. Explain the operation of online-UPS with relevant block diagram. (12) [CO2]
   b) Define and classify tuned amplifier. Explain the principle of operation of a transformer-coupled push-pull amplifier circuit. (10) [CO3]
   c) How undammed oscillation can be obtained? Design a second-order high pass active filter with resonat frequency of $5KHz$ and closed-loop gain 50. (13) [CO4]