PROTECTION OF THE INTER-TIE BETWEEN AN INDUSTRIAL COGENERATOR AND A UTILITY

by

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DECLARATION

I hereby declare that this thesis is a record of work undertaken by

myself, that it has not been the subject of any previous application

for a degree, and that all the sources of information have been duly

acknowledged.

During this research the following conferences were attended:

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In The Name of God
Most Gracious Most Merciful

ABSTRACT

PROTECTION OF THE INTER-TIE BETWEEN AN INDUSTRIAL COGENERATOR AND A UTILITY

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The work presented in this thesis is concerned with the development of a microprocessor based technique to detect and locate symmetrical and unsymmetrical faults on the interfacing network of a utility interconnected industrial cogenerator system; and to identify the type of the detected fault.

In order to provide operational flexibility and supply security to such an interconnected industrial cogenerator plant, fault location is regarded as being of prime importance. Current protection practices using conventional technology for this sort of interconnected cogeneration system were reviewed.

A relay coordination study was carried out on a simulated utility interconnected cogeneration system. This resulted in identification of the problems and limitations of the application of standard IDMT relays for overcurrent protection of such a system.

A review of digital protection, and its various algorithms, was undertaken. This provided the basis for a rational choice of algorithm for the proposed new technique.

The sequence of functions of the protection scheme's algorithm, based on the proposed technique, can be presented in brief as follows: First, phase currents at selected positions on the system are sampled. The positive phase sequence (pps) currents at those positions are then obtained in digitised form from the sampled phase currents. Then, these pps currents, containing fundamentals along with other harmonics and dc offsets, are used in a Fourier filtering algorithm to extract only fundamental components in rectangular forms. Signs of imaginary parts of these components are then used to determine the directions of pps currents at the selected positions. The industrial bus voltage is used as the polarising reference. Finally these directions are used in a fault detection and location subroutine to determine the location for any fault under such condid tions. After detecting a fault and locating its position, the type of fault is determined from off-line analysis of the postfault phase currents. The analysis is based on identifying the phases carrying the maximum fault current and checking the presence of zero sequence current.

The proposed protection scheme has been tested on a computer simulated system which consists of a utility interconnected to an industrial plant with cogeneration. The performance has been found to be satisfactory for all kinds of solid and low arc resistance faults anywhere on the interfacing network between the systems.

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INTRODUCTION

1.1 General

Energy resources are limited and finite in this world. Gradual exhaustion of cheap energy sources and its consequences on the society are becoming more serious worldwide. The cost of all forms of energy including coal, natural gas, fuel oil and electricity has increased several fold in the last 15 years [1]. The cost of electricity is expected to increase rapidly in the near future as the costs of fossil fuels continue to increase. In recent years, shortterm disruptions have been experienced by some oil and natural gas supply industries due to gradual decrease in reserves, which raise the fear about the long-term availability of several fossil fuels. There is, therefore, a developing energy crisis. Fortunately, it has been recognised in many countries that energy conservation policies must play a vital role in helping to slow down the rate of exhaustion of fossil fuel resources [2]. Subsequently, efforts are being made to develop technologies in order to recover as much energy from waste, unconventional and renewable sources as possible [3].

1.2 <u>Dispersed storage and generation</u>

The term "Dispersed Storage and Generation (DSG)" is used to describe small scale generation, usually ranging from 5 KW to 80 MW, from solid waste or renewable energy sources. It is also known as

Private Generation. Available renewable energy sources include hydro, wind, wave, tide, solar, geothermal, biomass and urban waste [4-6]. Although renewable energy sources are characterised by low energy concentration per unit surface area of sea and land, they offer attractive features like inexhaustibility, enormous theoretical potential and ecological cleanliness in particular. Our planet is proceeding towards the possible catastrophic consequences of global warming due to large-scale use of fossil fuels and nuclear pollution from the use of nuclear fuel in conventional power plants [3]. With the growing concern over the energy crisis and global warming, effective utilisation of all possible renewable energy sources for electricity generation is being promoted worldwide [7].

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1.3 <u>Cogeneration</u>

The term "cogeneration" is rapidly becoming familiar to engineers in manufacturing and power supply industries. The process of sequential generation of energy mainly in two forms, heat and electricity, from a common energy source is called cogeneration [8,9]. It is also known in the industry as combined heat and power (CHP) [10,11]. Cogeneration is not a new technology. It was recognised as an economic means to recover waste heat energy for electric power generation and was prevalent at the turn of this century, when a great majority of electric generating capacity was on industrial sites. This was primarily because public electricity supply was unavailable or costly. Introduction of a reliable and reasonable service in the mid 1900's, together with the availability of cheap fuels, brought

about a decline in the growth of industrial cogeneration [12-14].

Since cogeneration is a sequential process, with the waste heat from one process being captured for use as an energy input in another process, it requires firstly, some amount of common physical plant space for the two processes and secondly, a sharing of the energy content of the input fuel. This joint system can reduce energy input to 10 - 30% below that required by separate systems to produce the same outputs. Total system efficiency can approach 90% [15]. On the other hand, in conventional power stations employing condensing turbines, only approximately 35% of the fuel input is received in the form of electric energy. The remainder of the fuel calorific value is lost [10].

With the increasing necessity for energy conservation and escalating costs for building new utility power plants, industrial cogeneration along with DSG is being encouraged worldwide. Industries likely to offer good cogeneration potential include paper, cement and fertilizer mills as well as many food processing and chemical plants, which produce steam for their production processes and use the heat energy of waste or excess steam for electricity generation.

1.4 <u>Interconnection of industrial cogeneration with utilities</u>

1.4.1 Configuration of the interconnection

The industrial cogeneration may be interconnected with a utility in different ways [16-20]. However, the interconnection is almost

always made through an interface transformer, which provides an impedance buffer between the two systems. The voltage level, at which the interconnection is made, depends [17] mainly on the maximum electricity demand of the industrial plant; whereas the configuration of the interfacing network depends on electricity demand, cogeneration capacity and the degree of supply security required by the industrial plant. Fig. 1.1 shows different modes of interconnection. A common form of utility-industrial cogeneration interconnection is shown in Fig. 1.1(a) where the customer busbar is interconnected with a utility through a single link. The cogenerator is directly connected to the customer busbar which also supplies the industrial loads. However, the supply security of the configuration, shown in Fig. 1.1(a), can be improved by sectionalising the customer busbar and putting the essential load and cogenerator in one section and the non-essential load in other as shown in Fig. 1.1(b). In the case of a heavy industry, which requires a very reliable power supply, the interconnection is made through a multiple link as shown in Fig. 1.1(c). In the case of low-scale industrial cogeneration, the cogenerator is connected further down from the interfacing point at a low voltage busbar as shown in Fig. 1.1(d).

1.4.2 Advantages of parallel operation

From the previous discussion it can be seen that industrial cogeneration is economically justified by the value of electrical energy generated. Industrial cogeneration, operating in parallel with a utility, becomes even more economical compared with its stand-alone

operation, since the costly additional steam generators, required to augment the steam supply to the turbogenerators, can be eliminated by using the utility as a makeup source [16].

In parallel operation, the cogeneration plant can be used to reduce the peak demand on the utility in order to achieve a more attractive tariff. Parallel operation also provides the industry with a facility to sell profitably its excess electric power to the utility. In addition, it increases the power supply security of the industrial plant by using the utility as a redundant source. Furthermore, it increases the flexibility and ease of plant operation, which can be translated into significant economic benefit [21,22].

1.4.3 <u>Factors influencing the interconnection</u>

Although the addition of cogeneration facilities to an industrial site and, in particular, the interconnection of these facilities with a utility for parallel operation is being encouraged in recent years for both economic and supply security reasons, it presents several concerns for the utility. Review of literature [4,6,17,22-28] reveals that these concerns include safety, power quality, reliability, choice of protection scheme, switchgear capacity and relay coordination, planning, operation and metering systems and rate structure. The industrial plant may have a slightly different set of concerns such as, safety, protection of cogeneration system, interconnection cost and impact on production.

Safety of personnel

Safety of maintenance personnel is of paramount concern. Utility maintenance personnel are always required to follow a set of safety work rules laid down by the utility. The interconnection of industrial cogenerators for parallel operation with the utility will make the standard safety work rules quite inadequate. For example, when the tie line is opened by the utility- owned circuit breaker for a fault on the utility, the industrial cogenerator may remain connected to the customer busbar, energising the downline of the tie. Having mistakenly deduced from the open state of the utility circuit breaker that the tie was de-energized, utility personnel may start maintenance work. This could be a potentially dangerous situation.

Another safety concern is the possibility of energising an isolated utility circuit from the cogenerator. Closure would endanger the public and utility workers and others who have determined that the circuit was de-energized and were in contact with the circuit.

Safety of equipments

Although the use of autoreclosure is very common in utilities in order to improve the service continuity, a high speed autoreclosing device on the utility-industrial tie can be a serious problem for both the utility and the industrial plant. For example, due to temporary faults on the utility, the autoreclosure may reclose the utility on to the industrial cogenerator out of phase. This can

create dangerous torque transients on the rotating machines and consequently damage the machines within the industrial plant.

Another concern is the resonance between the power factor improvement capacitance and the inductance of the cogenerator winding under islanding condition. This resonance can create a dangerous overvoltage on the isolated system during a single line to ground fault. Some investigators [27] have found that conventional sensing is not fast enough to avoid equipment damage. Islanding occurs when the utility is disconnected, usually as a result of a fault, from the rest of the industrial system and the capacity of the industrial cogenerator is adequate to carry the isolated industrial load.

Power quality

Power quality is assessed by the degree of fluctuation of voltage and frequency, amount of harmonic content and power factor. The utility is obliged to maintain its system voltage and frequency within certain tolerances so that customer equipments function efficiently and reliably. The utility system, therefore, expects that the cogenerator power, sold to the utility, will be within the acceptable tolerances.

Injection of harmonics by the cogeneration system is a concern for the utility. These harmonics distort the power signal of the utility system. Harmonic currents can cause improper operation of earth fault and other protective relays and sensitive electronic equipment [15]. Saturation and imperfect flux distribution in the cogenerator winding may be the source of harmonics in the industrial system.

Low power factor may be another problem [15]. It can cause large voltage drop in supply circuits, an increase in power loss and equipment overheating. Thus the utility expects that the industrial system should be operated at a good power factor i.e. near unity. The utility may impose some penalty in its billing agreement for low power factor.

Reliability

The reliability of the utility service is important to the cogeneration scheme as well as to the utility itself. Being one of the customers of the utility, the owner of the cogenerator desires a reliable service. It is, therefore, the responsibility of the cogenerator owner to ensure that his equipment does not affect the reliability of the utility by causing unnecessary interruption. This consideration may influence the selection of equipment operating points and the equipment protection schemes.

Utility system reliability is also influenced by the location of the cogenerator interconnection with the utility. If the interconnection is made at transmission level, the interruptions of cogenerator service have greater impact than those at a distribution level. Consequently, the utility may require even more stringent protection of the cogenerator in order to protect other customers downstream of the cogenerator.

The cogeneration capacity also has impact on the reliability of

utility system. If the output capacity of the cogenerator is much smaller than the plant load, disturbances created by the cogenerator may not have significant impact on the rest of the plant and on the utility. However, if the cogenerator output capacity approaches or exceeds plant load, the cogenerator's disturbances affect significantly both the plant and the utility. This will usually necessitate a more stringent protective scheme.

Choice of protection scheme

In an industrial cogenerator-utility interconnected system, both the utility and the cogenerator need to protect their respective facilities and personnel from any damage and injury that could be caused by the fault on the utility, on the interface or by cogenerator misoperation. However, it is a difficult task to choose an appropriate quality and quantity of protection and setting of relay trip points. This is due to the fact that the protective scheme should be satisfactory to both systems which may have conflicting operating requirements. For example, the cogenerator would ideally like to have wide limits of operation so that the generator can operate with infrequent disconnections. In addition, the cogenerator owner would prefer to protect his equipment at the least possible cost. On the other hand, the utility would not compromise with the reliability of its service. As a consequence, it requires a greater margin of protection for its facilities in order to maintain service to other customers.

Switchgear capacity and relay coordination

The addition of a cogeneration scheme to an industrial system is a concern for the utility due to the fact that the cogenerator increases the fault level as well as the reactance to resistance ratio of the overall system. This may necessitate redesigning of the intertie substation and its switchgear equipments. For instance, the ratings of fuses, circuit breakers and intertie busbars may require to be upgraded in order to cope with the extra fault currents, contributed by the cogenerator. This excess fault current may also disturb the coordination of overcurrent relays on the system. This is discussed in the following paragraph.

Without cogeneration facilities the industrial system imports all its required electric power from the utility. Thus it can be considered as a single end fed radial distribution system. The extent of outages on this sort of radial system is minimised by opening only the protective devices closest to the fault. This can be achieved by placing successively more sensitive overcurrent protective relays on the circuit as the distance of the relays from the power source increases. The pick-up current of each relay is determined by the minimum fault currents at relay locations. When a cogenerator is added to the system, the fault current is increased significantly throughout the system. As a result, the coordination of the overcurrent relays may be lost and this leads to maloperation of the relays. Thus, the presence of cogeneration may impose requirements on the utility to modify its coordination of protective devices.

Planning and operation

The presence of cogeneration may affect the utility planning for the following reasons. Firstly, the traditional operating strategies of cogeneration facilities are governed by factors, which may be quite different from those of utility. The basic philosophy behind the design of a public supply system is to meet the growing and periodically varying electrical loads; whereas, the cogenerator's concerns lies primarily with meeting thermal demands of manufacturing processes and then, as a secondary consideration, the electrical power generation capabilities. Secondly, the assumption of unidirectional power flow from utility to consumer may no longer be valid.

Utilities need to account for the deviations from their expected load surveys and load factors caused by cogeneration. Load surveys, which are used to determine the electrical demands of the utility at present and in the future, are the foundation of utility planning. Load factor reflects the utilisation factor (ratio of average use to peak use) of the utility equipments. Both of these factors are affected by cogeneration, which is usually not planned for and displaces some electrical demand as well.

The interconnection of industrial cogeneration with a utility presents operating problems to both the utility and industrial site. The utility's operating problems are discussed first, followed by the operating problems of the industry. Firstly, cogeneration plant affect the operation of utility generation due to their base load mode of operation. This base load mode usually increases the utili-

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ty's daily unit commitment problems. Unit commitment is a technique to decide which of the available generators should start-up and shut-down over a given time horizon in such a manner that the demand and the spinning reserve requirement are satisfied and overall fuel cost is a minimum [29]. Secondly, the utility experiences a significant decrease in operating flexibility. Base load cogeneration effectively removes the constant load that the utility generators would normally serve and thus contributes nothing to serving the variable load of the utility. Thirdly, the worst operating problem arises in the case of a cogenerator importing power from the utility during its peak period and exporting to the utility only during the off peak period (termed off peak dumping). In these circumstances similar problems, as discussed before, occur, but a much sharper load pickup is required by the utility and the total amount of load swing is effectively increased. Furthermore, cogeneration affects fuel planning, voltage control, system outage planning and system security analysis of the utility.

As mentioned previously, the primary factor involved in building a cogeneration facility is normally to meet internal demands (thermal and electrical) economically and efficiently. Depending upon the flexibility with which a cogenerator is designed, increase or decrease in electric power generation requested by the interconnected utility can cause disruption of steam flow and pressure provided for manufacturing process use. Typically, utility personnel may not be fully aware of these restrictions and tend to impose operational requirements upon the cogenerator as they would on one of their own

power stations. However, in a typical large cogeneration facility a combination of steam and gas turbines can be utilised to cope with this power demand variation after meeting the internal thermal and power demands.

Metering systems and rate structure

Metering systems, which are based on unidirectional power flow i.e. from utility to customer are required to be modified when a cogeneration scheme is installed within the industrial plant. There should be separate metering systems to measure both imported and exported electric energy, which may have different rates. It is sometimes difficult to find a suitable rate satisfactory to both parties, particularly when the cogenerator wants to buy energy from the utility during its peak period and wants to sell during off-peak period.

1.5 <u>Current practices for protection of industrial</u> cogenerator-utility <u>interconnected system</u>

1.5.1 Overview of the protection

The main objective of protective relaying is to detect abnormal conditions and isolate the problematic areas. The design of a relaying scheme for the protection of a utility interconnected industrial system, without cogeneration facilities, is based on unidirectional power flow, i.e. from the utility to the industrial plant. Overcur-

rent protection alone can be considered sufficient if the interconnected industrial system is relatively small. If, however, the industrial system is extensive, high speed differential protection for the link becomes essential as a primary protection, while overcurrent protection remains as a backup [30].

Addition of cogeneration facilities to the industrial system may result in bidirectional power flow in the interface link, according to the cogeneration capacity, and the variation of the industry's electric demand under normal operating conditions. This complicates the protective scheme of the interface. Since the configuration of the interconnection depends upon the demand and supply security requirement of the industry, the protective schemes will be different for different requirements. Several publications, Engineering recommendations and Technical reports [5,6,19,20,27,31-35] have analysed and recommended protective schemes for this sort of bidirectional power flow interface. The most common additional relays required at the intertie include over and under-voltage relays, over and under-frequency relays, a synchronising relay and lockout relay.

For a fault on the utility or on the intertie of an interconnected system, where the electrical output of the cogenerator is very small compared to plant demand, simultaneous disconnection of the tie and the cogenerator is the present common practice. This avoids the possibility of reclosing the utility on to the cogenerator out of phase. This practice can be justified by the fact that the cost incurred by the extra switchgear and protective relays for retaining the cogenerator in the isolated condition is not economical. Howev-

er, if the cogenerator capacity is comparable to the plant demand and complete power failure results in a threat to the industrial plant's profit, it might be preferable to allow the industrial cogenerator, with a proper load shedding scheme, to run as an isolated system to meet the critical load. This, of course, requires additional relays and switchgear as mentioned before. In addition, it requires a change in circuit breaker controls and some sort of interlocking between the utility breaker and the customer breaker at the interface link. This will be discussed in the next section.

When a short circuit occurs on an industrial cogenerator-utility interconnected system, both the utility and the industrial system contribute to the fault current. Therefore, both the utility and the cogenerator will have to be protected from possible damage caused by the fault. The protection scheme for this sort of interconnected system can be divided into the following three parts. Firstly, if the fault occurs on the utility, the fault should be detected and isolated by the primary protection of the utility. However, the industrial system must have the provision to protect its equipment in the event of the utility relays and breakers failing to detect and isolate the fault. This is called backup protection for the industry. In this kind of backup scheme, relays are provided on the industrial system which detect a fault on the utility and disconnect the generator (or alternatively, the link between the industrial system and the utility) if the utility system fault has not been cleared by the utility relays and breakers within a predetermined period of time. Secondly, when a fault occurs on the industrial system, the fault should be detected and isolated by the primary

protection of the industrial site. However, the utility must be provided with a backup protection scheme to safeguard against failure of the industrial primary protection. This is known as backup protection for the utility. Finally, when a fault occurs at the interface link, the fault should be isolated by the protection scheme of the link.

Fig.1.2 [19,20,36] shows a typical example of a protective scheme for a bidirectional power flow industrial cogenerator-utility interconnection. The scheme combines all the aforementioned considerations and allows the cogenerator to run as an isolated system in the case of a utility or interface link fault. The relaying scheme will be discussed in the following sections with reference to Fig. 1.2.

1.5.2 <u>Protection of the interface</u>

Since the interface link connects the two systems together for parallel operation, the protection of the link i.e. the interface transformer is extremely important. The interface transformer should always be chosen with adequate capacity to handle the total load of the industrial plant irrespective of direction of power flow in the link. Taking this into consideration, the protection of the interface transformer is, by convention, provided with a percentage differential relay (87T) and Buchholz relay (63). The differential relay provides sensitive and instantaneous protection for faults occurring in the zone between the differential connected current transformers near the utility side circuit breaker (A) and the

customer side circuit breaker (B). Faults within this protection zone are cleared by the breakers A and B. A harmonic restraint feature should be included in the percentage differential relay in order to prevent false tripping when magnetising current inrush occurs. Local backup for the transformer differential relay failure is provided by the time overcurrent relay (51) fed from the CTs of the differential scheme.

The Buchholz relay operates in response to a sudden rise of pressure in the transformer tank. This sudden pressure rise is caused by rapid vaporisation of the insulating liquid during faults within the tank. However, the relay does not operate with a gradual rise in internal pressure caused by normal load variation or by changes in ambient temperature. Moreover, if a breather device is fitted with the transformer tank, it allows air flow in and out and thus prevents slow pressure changes.

The main purpose of including the customer breaker B in the protection scheme is to provide the facility of isolated operation of the industrial site under fault conditions on the utility or on the interface link. In addition, some form of interlocking between the breakers A and B is required to make isolated operation safe. For example, for faults on the utility system or on the interface link, the breaker A is opened first followed by breaker B. To close breaker B, the following two requirements must be met sequentially: first, breaker A must be closed and then the plant cogenerator must be synchronised with the utility system by changing its speed and field preferably by autosynchroniser. This interlocking arrangement

will alleviate the problem caused by adding a autoreclosing facility to the utility breaker A.

The function of the lockout relay (86) is to lock the breaker (or autoreclosure) A in the open position after being tripped by a permanent fault on the utility or on the interface link. This also ensures safety of the maintenance personnel.

1.5.3 <u>Protection of the industrial plant</u>

Before going to a discussion of backup protection for the industrial site, consider first its main protection. The busbar differential relay (87B) is provided to detect faults on the customer busbar, to which the cogenerator is connected, and initiate the disconnection of both the utility and the cogenerator by breakers A and C respectively (see Fig. 1.2). The local backup protection of busbar differential relay is provided by a time overcurrent relay (51B).

Phase faults on the feeder are detected by the instantaneous and phase time overcurrent relays (50/51) and ground faults by the instantaneous overcurrent ground fault relay (50GS).

Internal faults in the industrial cogenerator are detected by the generator differential relay (87G). The voltage controlled time overcurrent relay (51V) in the generator circuit provides a local backup for the generator differential protection. The generator is protected against motoring and rotor overheating by a reverse power relay (32) and negative phase sequence relay (46) respectively. All the generator protective devices described above actuate breaker C

in order to disconnect the generator in fault conditions.

Having provided adequate protection for faults within the industrial system, it must also be protected against faults on the utility side which may remain undetected and uncleared by the utility protection scheme. A directional time overcurrent relay at the link is not suitable to provide backup protection for the industrial system for faults on the utility system for the following reasons : firstly, if the link carries power in both directions under normal operating conditions according to contract between the two parties (utility and industrial customer), there will be no unique information (i.e. fault or normal operation) in the direction of current flow at the link. So a directional overcurrent relay is ineffective. Secondly, under a unidirectional power flow contract (from utility to industry), any current flowing from industry to utility will indicate a fault at the utility. But the fault current at the relay after a predetermined period of time may reduce to less than its pickup value due to dynamic interaction between the industrial generators and motors during the fault [20]. However, a second zone delayed distance relay (21-2), shown in Fig. 1.2, can suitably provide the backup protection in this situation.

When the interface transformer has a delta connected high voltage winding and a wye connected low voltage winding, as shown in Fig. 1.2, there will be no ground (zero sequence) current in the high voltage winding for a ground fault on the utility. However, the utility's remote end relay will detect it and isolate the circuit from that end and a transfer trip signal will open the breaker A as

well. To provide backup protection for the industrial site for this type of utility ground fault, a zero sequence voltage relay, also called ground detection relay, (59G) is used.

1.5.4 <u>Protection of the utility</u>

The utility must have adequate protection to safeguard against faults within its own system. This is not the concern of this work and thus will not be discussed. However, the utility is concerned to protect its equipment from faults on the industrial system, which are not cleared by the industry's protection. Backup protection for the utility in the event of industrial system faults could be as follows.

Firstly, an overcurrent relay (50/51) at the top of the link, shown in Fig. 1.2, provides backup for the utility. The settings of the relay are chosen to coordinate with the phase time overcurrent relays on the busbar and on the feeder. Secondly, backup protection for ground faults on the industrial system is provided by the time overcurrent ground relay (51TG) fed from the CT in the transformer neutral connection. This relay must be coordinated with the ground relay at the busbar (51BG) but need not be directional because it will not respond to ground faults on the utility. Finally, in order to provide backup relaying at the far end of the utility supply line, distance relays could be a suitable option. An instantaneous first zone relay should be set to reach into but not through the interface transformer, and the second zone relay should be set to

reach through the interface transformer to provide backup for faults on the industrial busbar or on the feeder. This option, however, is not shown in Fig. 1.2.

1.5.5 Choice of grounding

The grounding plays a vital role in the design of an industrial system as well as its earth fault protection scheme. However, there is no single best grounding practice which can meet the requirements of every plant. A suitable grounding system depends on the operating environment of the plant. For instance, when the utility is the sole source of power for the industrial site, grounding could be based on long standing traditional practices. Secondly, when an industrial system, with its cogeneration scheme, is completely independent of the utility, the user may choose a unique procedure for grounding. However, if both systems are interconnected for parallel operation, neither of the above grounding choices may be ideal [37]. In the case of a utility interconnected industrial cogenerator, the following factors will have an impact on the decisions for grounding. These include fault current, harmonic current and overvoltage [16,38]. Each one of these factors influences the others. For example, high ground fault current, as in the case of a solidly grounded system, can cause damage to equipment but reduces the risk of overvoltage. On the other hand, too much limit on ground fault current may result in excessive overvoltage which may cause insulation failure.

Fault current

Generally, the generator windings are braced to withstand the mechanical forces resulting from a bolted three phase short circuit at the machine terminals. Generators with solidly grounded neutrals will usually have phase to ground fault currents in excess of their maximum three phase fault capability [39]. In addition, as the number of ground sources in the system increases, the total ground fault current also increases. In a utility's transmission system, solid grounding is the common practice which facilitates protective relaying for selective operation. In medium or low voltage industrial systems, ground fault current is limited to less than the three phase fault current. This is done by adding impedance in the neutral to ground circuit.

The choice of the impedance and location of the ground source may become a difficult task. When a plant owner wants to continue production operations under ground fault conditions, which is however a very rare case, the value of the neutral to ground impedance should be high enough to limit the ground fault current to a low level. This, of course, aggravates the problem of system overvoltage, fault detection and relaying. On the other hand, very low impedance in the neutral can result in high fault current, causing equipment damage but easing fault detection and protective relaying. Therefore, the value of the neutral to ground impedance should be high enough to limit the fault current to less than a dangerous value, and at the same time low enough to give adequate fault current for easy fault detection and relaying.

Because of the added complexity in relay selectivity and determination of ground fault current with multiple grounding, a single ground source is preferred. Two easy options are available for providing a single ground source in a utility interconnected industrial cogeneration system: either at the neutral of the cogenerator or at the neutral of the delta-wye connected interface transformer [38]. The disadvantage of the first option is that the industrial system becomes ungrounded in the case of cogenerator disconnection. The second option is better than the first one in the sense that the system ground remains intact even after the cogenerator disconnection. However, disconnection of the interface transformer leaves the industrial system again ungrounded. Therefore, grounding the neutrals of both the cogenerator and the interface transformer is the possible option to avoid the chance of system ungrounding under any circumstances.

Harmonic current

Core saturation and imperfect winding and flux distribution are the main causes of generation of third and other odd harmonic currents in the generator. Depending on its design, the industrial cogenerator may produce up to ten percent third harmonic current [39]. Two or more industrial cogenerators, with their neutrals grounded, running in parallel may produce excessive third harmonic currents. It may, therefore, be necessary to restrict the neutral grounding to a single machine and provide automatic transfer facilities of the

generator neutral to another machine in the event of the selected machine being tripped. In addition, earthing arrangements must be designed such that the operation of the utility's protection system is not adversely effected [34].

1.6 <u>Objective of the research</u>

It has been mentioned previously that industrial cogeneration is becoming increasingly attractive as a result of the developing energy crisis. Parallel operation of industrial cogeneration with a utility is even more attractive both economically and technically. Parallel operation helps to reduce the overall energy expenditure as well as improving operational flexibility and supply security for the industrial site. However, it necessitates a stringent protective scheme for the interconnected system, particularly the interface link. The protection scheme becomes even more complex and expensive when the interface link is meant to handle bidirectional power flow under normal operating conditions. It is important to note that any industry, having a considerable amount of cogeneration capacity, will obviously prefer to run its system isolated in the event of faults on the utility or on the interface link. If, however, the fault occurs on the industrial busbar, to which both the utility and cogenerator are connected, the industrial site is left with only one option i.e. shutdown the entire system. It is, therefore, essential to locate faults on the system in order to achieve aforementioned flexibility.

Fig. 1.2 shows a typical example of a complete protection scheme,

which can detect, locate and isolate the faults, for an interconnected system where the interface link handles power in both directions. Fig. 1.2 also illustrates the complexity and gives an impression of the cost involved in the protection scheme. Seeking a comparatively simple, cheap, fast and reliable protection scheme to replace the complicated and expensive existing version is the theme of this research work.

The objective of this research is to develop a microprocessor based new technique to detect and locate symmetrical or unsymmetrical short circuit faults anywhere on the interconnected system. A single protection scheme based on this technique will be able to replace all differential zone protection, reverse power protection of the cogenerator and the feeder main protection, and consequently becomes cheap. The technique has been tested on a computer simulated system and the results show that such faults can be detected and located well within one cycle after the fault inception.

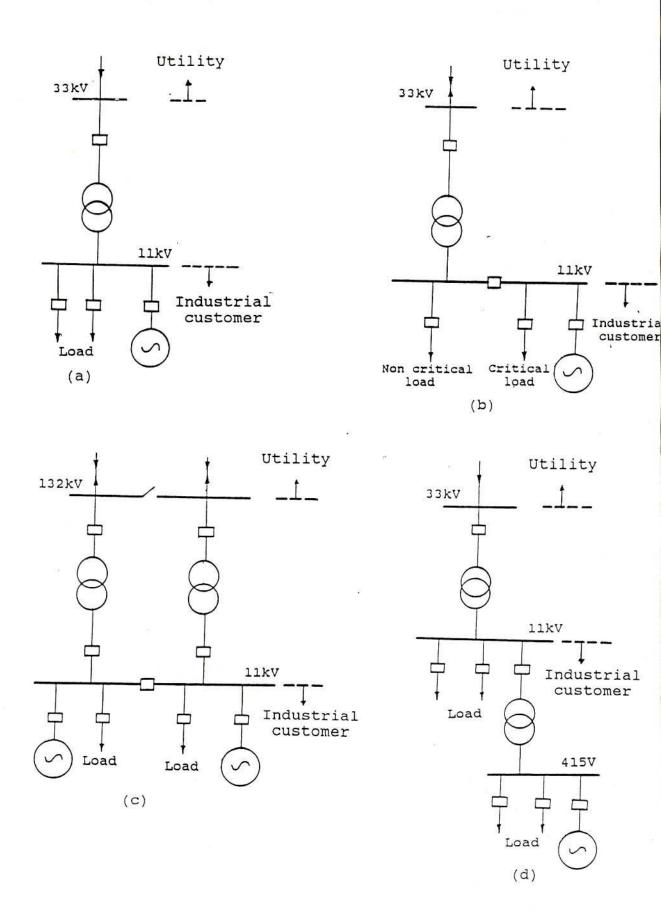


Figure 1.1: Typical examples of mode of interconnection between utility and industrial cogenerator.

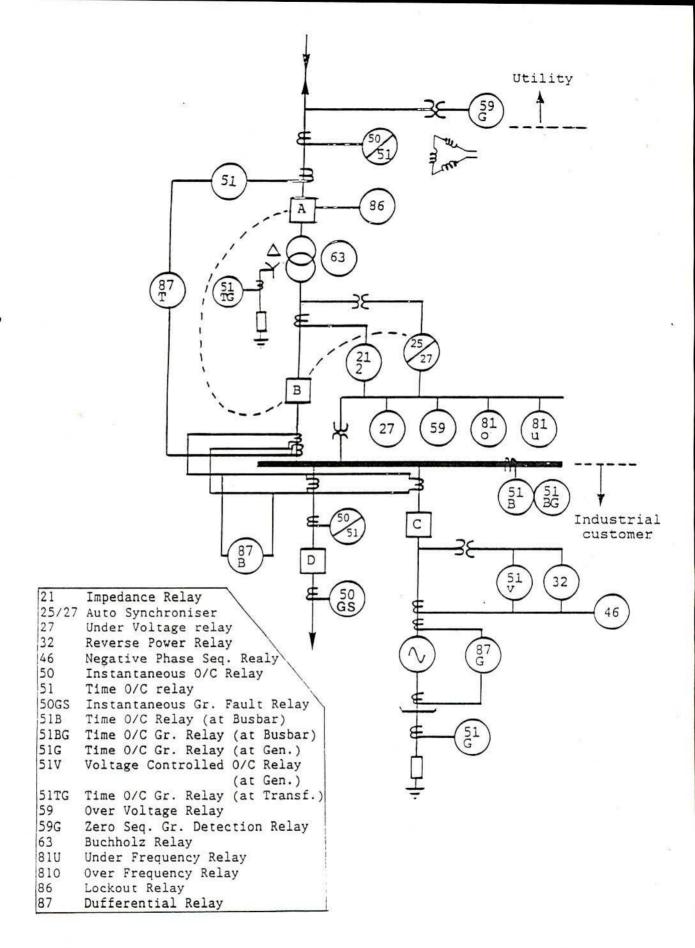


Figure 1.2: Typical example of a protective scheme for a bi-directional power flow interface.

CHAPTER TWO

COORDINATION STUDY OF IDMT OVERCURRENT RELAYS ON A SIMULATED INDUSTRIAL COGENERATOR-UTILITY INTERCONNECTED SYSTEM

2.1. <u>Introduction</u>

Overcurrent protective systems have evolved from the basic principle of protection against excess current. Overcurrent protection is quite different from overload protection. The operation of overload relay depends on a time which is related to the thermal capability of the plant to be protected. On the other hand, overcurrent protection should function only on system faults [36]. There are various overcurrent relays in that the correct coordination is obtained by grading either time or overcurrent or a combination of both time and overcurrent. The common aim of all the relays is to achieve correct discrimination i.e. selection and isolation of only the faulty section of the power system network. There are, however, disadvantages with time or current grading alone. Firstly, in the case of discrimination by time alone, the disadvantage is due to the fact that the more severe faults are cleared in longest time. Secondly, discrimination by current alone can be applied only where there is an appreciable impedance between the location of two relays concerned.

Because of the limitations imposed by the independent use of either time or current for discrimination, the combination of both time and current features, called inverse definite minimum time (IDMT), has

evolved. IDMT relays are widely used for the overcurrent protection of electric power systems due to their simple principle and low cost. They are used to provide main protection for radial distribution system and back-up protection for expensive interconnected systems, where the primary protection is provided by unit or distance schemes. Although IDMT relays cannot identify a fault zone, the discrimination between the adjacent protection zones can be achieved by adjusting the plug setting and time setting multiplier [40]. However, there are limitations in the application of these relays. First, they do not provide all protection requirements of power systems. Secondly, satisfactory grading cannot always be achieved for complex networks. With a view to identifying these application difficulties of standard IDMT relays, a relay coordination study was conducted on a simulated utility interconnected industrial system, having cogeneration facilities. This chapter describes the application of these relays to the simulated system and presents the results of the study.

Without cogeneration facilities the industrial system imports all its required electric power from the utility. Thus, it can be considered as a radial distribution system with single-end feeding. Hence, the fault level at any point on the system decreases as the point moves away from the feeding end [41]. Various parts of this radial system can be protected by using standard IDMT relays at suitable locations. Proper time discrimination between the operation of the relays at different locations can be ensured easily under this situation by choosing the appropriate relay settings according

to the fault level.

The addition of cogenerators to the industrial system causes an increase in fault level throughout the system. Consequently, the relay coordination in the entire system could be disturbed and, more importantly, discrimination between some of the relays is totally destroyed. Therefore, the settings of the relays must be modified to bring back the proper coordination with the increased fault level. However, this study shows that it is difficult to obtain correct discrimination, particularly between the cogenerator relay and feeder relays further down from the cogenerator.

2.2. <u>IDMT relay characteristic</u>

IDMT relays with different operating characteristics are available to suit different requirements. Typical operating characteristics in use are standard inverse, very inverse and extremely inverse [36]. The standard IDMT relay characteristic, shown in Fig. 2.1, is used for this study. The relay has two controls: plug setting and time setting multiplier (TSM). The plug setting is a device used to provide a range of current settings at which the relay starts to operate. The setting ranges from 50% to 200%, in steps of 25% of the relay rated current. The TSM is a means of adjusting the movable backstop which controls the travel of the disc and thereby varies the time at which the relay closes its contacts for given values of fault current. It ranges from 0 to 1 in steps of 0.05 [42]. The characteristic curve moves horizontally with the variation of plup setting and moves vertically with the variation of FSM.

The standard IDMT relay characteristic is modelled mathematically by using the following equation , given in BS 142 [43], considering TSM at 1:

$$t = 0.14/(I^{.02}-1)$$
 (2.1)

where t is the characteristic operating time and I is the plug setting multiplier. To obtain the actual operating time of a relay with TSM other than 1, as is usually the case, the characteristic operating time obtained from eqn. (2.1) is multiplied by the TSM of the relay.

2.3. Relay settings

For proper coordination between various relays on a radial feeder, the plug settings must be adjusted such that each will operate for all short circuit faults in its own section and should provide a back-up protection for short circuits on the immediately adjoining section. Their time settings must be just long enough to permit the relays in the faulted section to work first. On a radial feeder each relay backs up the one in the next section further from the source so that the time current characteristic of the back up relay should be immediately between the characteristics of the relays on each side of it [42]. The settings of each relay are chosen in such a way that prevents any crossing of time current characteristics of different relays at all fault current levels.

2.3.1 Relay current setting

It is very important to choose the current setting adjustment at a value in excess of the nominal rating of the plant to be protected in order to maintain system stability under overloading and transient conditions. In overcurrent protection a load margin depends upon the user's choice as there is no generalised rule [44]. After selection of a load margin, the overload rating i.e. the maximum expected load of the plant is calculated. The primary current of the current transformer and the plug setting are chosen in such a way that their product, called relay current setting, is always greater than or equal to the overload rating. To give an example, a load margin of 30% is chosen for a plant having a nominal load current of 250 A. The overload rating of the plant will be 250(1+0.3) i.e. 325 A. Assuming 200 A CT primary current, the plug setting should be set at 175% to give relay current setting of 200 x 1.75, i.e. 350 A which is greater than 325 A, the overload rating [41].

2.3.2 <u>Time setting multiplier (TSM)</u>

For proper coordination between the relays, connected in series, on a radial feeder, the TSM of the relay farthest from the source should be set at a minimum value so that it operates at a minimum possible time. The TSM of the succeeding relays towards the source should be increased for selective operation. The time grading should be done at the maximum fault current because it will automatically give a higher selectivity at minimum fault current as its character-

istic curve is more inverse in the lower current region. The grading margin, i.e. the interval between the operation of two adjacent relays, is governed by the following factors [36,44]:

Circuit breaker interrupting time

In interrupting a fault, the circuit breaker must have completely interrupted the fault current before the discriminating relay ceases to be energised.

Overshoot time of the relay

Even after de-energization of a relay, its operation may continue for a little longer until any stored energy has been dissipated. For example, firstly, energy may remain stored in capacitors of static relay circuits. secondly, an induction disc relay will have stored kinetic energy in the motion of the disc. Relay design is directed to minimizing and absorbing these energies, but some allowance is usually necessary.

Errors

Relays and current transformers, being measuring devices, are subjected to some degree of errors. For example, the operating time characteristic of relays, involved in coordination, may have positive or negative errors. Current transformers may have phase and ratio errors due to the exciting current required to magnitize their

cores. In relay coordination, the setting is carried out assuming the accuracy of the calibration curves published by manufacturers, but some tolerance must be allowed to cover the expected errors.

Safety margin

After providing all the allowances, there might have a possibility that the discriminating relay just fail to complete its operation. Therefore, some safety margin is required to ensure a satisfactory contact gap of the discriminating relay.

The total interval between the successive relays required to cover the above factors depends upon the operating speed of the circuit breaker and the relay performance. At one time 0.5 sec was a normal grading margin. With the advent of modern fast circuit breakers and lower relay overshoot times, 0.4 sec is reasonable, while under the best conditions even lower intervals may be practical.

2.4. Grading procedure

The main objective of relay grading is that the relay closest to the fault should select and isolate only the faulted section of the power system in the minimum possible time, leaving the rest of the system undisturbed. If the relay fails to operate, the adjacent relay (i.e. back up relay) should operate after a period of time, called the discrimination time or grading margin. From a knowledge of the current transformer rating, plug setting and fault current flowing through the relay location, the operating time of a relay

can be evaluated by using the following basic equations [45]:

$$I_{rs} = I_{ct} \times PS/100 \tag{2.2}$$

$$PSM = I_f/I_{rs}$$
 (2.3)

$$t_{c} = f(PSM) \tag{2.4}$$

$$t_a = t_c \times TSM \tag{2.5}$$

where I_{rs} , I_{ct} , I_f are the relay current setting in terms of primary current, primary rating of the current transformer and fault current respectively. PS, PSM, TSM are the plug setting, plug setting multiplier and time setting multiplier respectively. t_c and t_a are the characteristic operating time and actual operating time of the relay respectively.

The grading procedure is best illustrated with reference to a radial distribution system shown in Fig. 2.2 [41]. In this system fault currents \mathbf{I}_{f1} and \mathbf{I}_{f2} , at points F1 and F2 respectively, are assumed to be known. Being farthest from the source, relay 2 is considered first in the grading procedure. Its time setting multiplier, TSM2, is set at a minimum value which allows sufficient relay contact travel to safeguard against the operation due to mechanical shock. Its plug setting, PS2, is chosen according to the procedure discussed in section 2.3.1. Having chosen these settings, its actual operating time, \mathbf{t}_{a2} , for a fault at F2 can be determined through the following steps. First, its relay current setting, \mathbf{I}_{rs2} , and plug setting multiplier, PSM2, are calculated using eqns. (2.2) and (2.3) respectively. Then, its characteristic operating time, \mathbf{t}_{c2} , corre-

sponding to PSM2 is evaluated from the standard IDMT relay curve, which is represented by eqn. (2.4) and shown in Fig. 2.1. Finally, the desired t_{a2} is obtained by multiplying t_{c2} by TSM2.

Having calculated t_{a2} , the next step is to determine the settings of relay 1 (i.e. its plug setting, PS1, and time setting multiplier, TSM1) for which the relay 1 will isolate the fault at F1 as soon as possible and back up the relay 2 for fault at F2. PS1 can be determined following the usual procedure. The TSM1, however, is evaluated through the following steps. First, the actual operating time of relay 1 , t_{a1} , for a fault at F2 is obtained by adding t_{a2} and a suitable grading margin, say 0.4 sec. Then, for the same fault at F2, the characteristic operating time of relay 1, t_{c1} , is obtained using eqns. (2.2), (2.3) and (2.4) as explained for the case of relay 2. Finally, the desired TSM1 is determined from t_{a1}/t_{c1} . Once the TSM1 is determined, its actual operating time for an adjacent fault at F1 can also be calculated following the procedure used for the case of relay 2.

2.5. The simulated system for coordination study

The simulated system used for the study of IDMT relay coordination is shown in Fig. 2.3, where an industrial system having cogeneration facilities is interconnected with a utility at 33 kV through a link. The link consists of a 500 meter long cable of 0.08 α/phase and a 40 MVA, 15%, 33kV/llkV transformer. The cogenerator is connected to the 11 kV customer busbar which supplies the load feeders. One of the

feeders, which is made up of a short cable of 0.04 \(alpha/\text{phase}\) and a 10 MVA, 10%, 11kV/3.3kV transformer, is connected to a 3.3 kV busbar. This feeds a 2 MVA, 3.3 kV motor load. Relays A, B, C and D are located as shown in the Fig. 2.3. The fault infeed capacity of the utility at 33 kV busbar is assumed to be 600 MVA. The study considers different sizes of the cogenerator varying from 10 MVA to a maximum of 40 MVA in 10 MVA steps. It also considers the case when the cogenerator remains disconnected from the industrial system.

2.6. Fault current calculation

The operation of an overcurrent relay depends upon the magnitude of fault current. It is, therefore, important to have a thorough knowledge of fault current distribution throughout the network in order to achieve correct grading [46]. In this study fault currents at all relay locations are calculated due to faults on the 33kV, 11kV and 3.3kV busbars with and without the generator connected to the industrial system. Since the relay grading is performed at the maximum system fault current, only three phase symmetrical faults are considered in this study. Prefault load currents are neglected. Since IDMT relays are relatively slow in operation and induction motors contribute to a fault only for the first three to four cycles from the fault inception [36], fault current contribution from the motor is also neglected. Generator fault current contribution is calculated using its transient reactance only. The decrement effect of generator fault current is also considered in the final part of the study.

2.7. Results of the coordination study

The coordination study of IDMT relays has been conducted on the simulated system, shown in Fig. 2.3. The following cases have been considered:

- i) Relay coordination with no cogeneration in the system.
- ii) Effect of addition of the cogenerator on relay coordination.
- iii) Coordination of relays A, B and D when a 40 MVA cogenerator is connected to the system.

2.7.1 Relay coordination with no cogeneration in the system

The first part of the study deals with the coordination of relays A, B and C when the cogenerator is assumed to be disconnected from the simulated system. Being farthest from the source the TSM of C is set at a low value of 0.1. The grading margin is chosen as 0.4 sec. The TSM of A and B, and operating times of A, B and C are computed using the procedure discussed in section 2.4. The time-current characteristics (TCC) of A, B and C are then computed on 3.3 kV base. These are presented graphically in Fig.2.4. It is evident from the TCC curves of Fig. 2.4 that the desired selectivity is maintained between the operation of the relays at maximum fault current and expected higher selectivity is obtained in the lower fault current region.

2.7.2 Effect of addition of cogenerator on relay coordination

In the second part of the study, an industrial cogenerator is included in the simulated system. The computations of TCC of relays A, B and C are repeated for different generator sizes, varying from 10 MVA to 40 MVA in steps of 10 MVA, while the initial plug setting and TSM of all the relays are kept unchanged. It is observed that the discrimination time between the relays decreases with the increase of generator size. The TCC of A, B and C are shown in Fig. 2.5 and 2.6 for the generator capacity of 10 and 40 MVA respectively. It is evident from Fig. 2.5 that the increased fault level, due to the addition of a 10 MVA generator to the system, reduces the initial grading margins between relays C and B and relays B and A from 0.4 sec to 0.36 and 0.27 sec respectively. These are further reduced to 0.31 and 0.13 sec respectively when the generator capacity is increased to 40 MVA as shown in Fig. 2.6. Since the grading margin between the relays is lost due to addition of the generator to the system, the fault discrimination capability of the relaying scheme is also lost. This means, both relays C and B operate for faults on the feeder protected by relay C. Similarly, B and A operate for faults on the feeder protected by B. In order to regain the proper coordination between the relays, their TSMs need to be modified. However, TSM of C is already set at the lowest value since it is farthest from the source. So, the TSMs of only B and A are modified. Fig. 2.7 shows the TCC of A, B and C with modified settings.

2.7.3 <u>Coordination of generator relay D with feeder</u> <u>relays A and B</u>

The final part of this study deals with the coordination of relays A, B and D for the condition of 40 MVA generation in the system. The settings of A, B and D are chosen in such a way that both A and D provide a back up protection for faults on the feeder, protected by B. The settings of D, in particular, are selected using the fault current contributed by the generator under transient condition. The study reveals that with the preceding settings, relay A operates correctly for the prescribed faults i.e. faults on the feeder protected by B, but D fails to respond when the decremental effect of generator fault current is considered. This is due to the facts that the utility's fault contribution remains fairly constant causing no problem to the grading between A and B. However, the available fault current at D, after the preset time delay, drops below its current setting and thus prevents the relay D to pick up. This can be better explained with reference to the decaying characteristic of generator fault current shown in Fig. 2.8. It shows how the generator fault current decays with time from its value, I_T , at transient period to its steady state value I_S , which is about one fifth of I_T . As stated earlier, $\mathbf{I}_{\mathbf{T}}$ is used for selecting the time setting of $\mathbf{D}.$ When relay D is supposed to operate after a period of time, according to the selected time setting, the actual fault current through the relay drops from I_T to I_S , which is, in fact, less than the current setting (i.e. 1.3 pu).

It is, therefore, difficult to choose a proper settings of D. For

example, if the time setting of D is made high enough to achieve proper selectivity with B, it does not respond at all in the event of the above described fault condition. On the other hand, if its current setting is made low, it will trip the generator on normal overloading condition. Due to these limitations it can be concluded that a standard IDMT relay is not suitable for generator overcurrent protection under these operating conditions.

A voltage controlled overcurrent relay is considered suitable for the generator backup overcurrent protection in this situation [36,47]. Fault conditions invariably cause a greater drop in voltage than normal overload. This fact has been utilized in a voltage controlled overcurrent relay. It is specially constructed to make its operating characteristics a function of both current and voltage. It is basically a low burden induction disc time overcurrent relay. The torque on the disc is controlled by a high-speed voltage element which has a predetermined dropout level [48]. When the applied voltage is above the pickup setting, the contacts in the voltage element remain in open position making the relay inoperative regardless of current magnitude. When the applied voltage falls below the dropout value, the contacts in the voltage element are closed. This enables the relay to produce torque and operate as a conventional IDMT relay. The advantage of this relay is that it can be set to pickup at less than generator full load current, and at the same time can be coordinated with the downstream feeder time overcurrent relay.

2.8. Conclusion

Simple principle and low cost have made IDMT relays popular for overcurrent protection of power systems, particularly radial distribution feeders. However, under certain circumstances, there are difficulties in the application of these relays. With a view to identifying these difficulties, a relay coordination study was conducted on a utility interconnected industrial system. The study shows that the addition of a cogenerator to the industrial system affects the relay coordination, and the higher the cogeneration size, the more is the disturbance with the coordination. In addition, the study identifies the problems and limitations in the application of IDMT relays for the generator backup overcurrent protection, in particular, due to decremental effect of generator fault current.

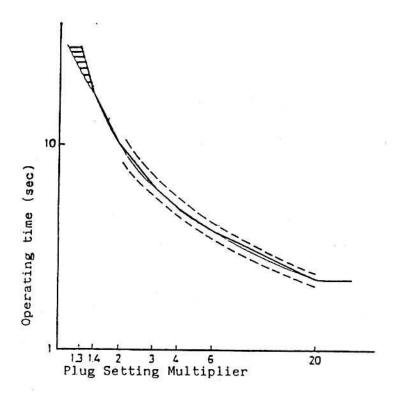


Figure 2.1: Standard IDMT curve (BS 142, 1983).

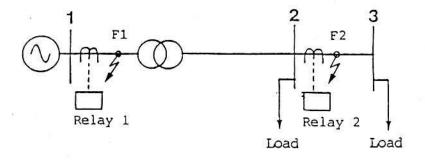


Figure 2.2: The radial distribution system.

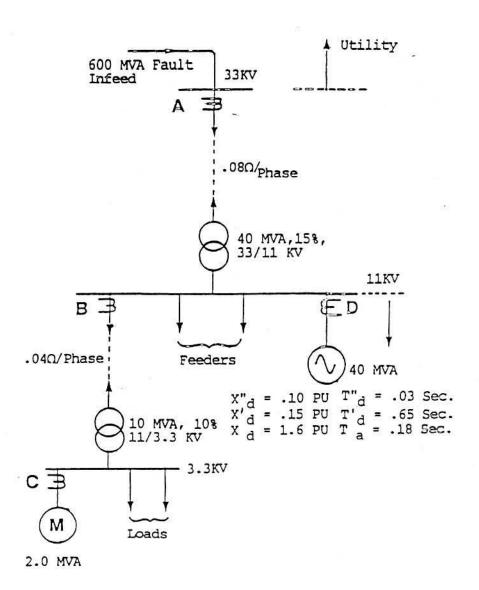


Figure 2.3: The simulated system.

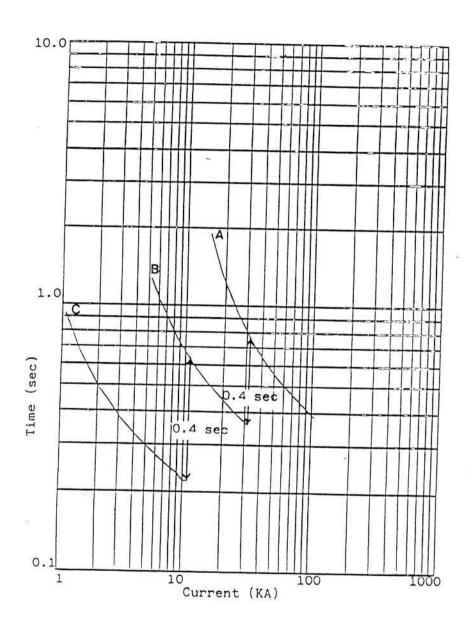


Figure 2.4: Time-current characteristics of relays A, B and C With the absence of cogenerator (on 3.3 kV base).

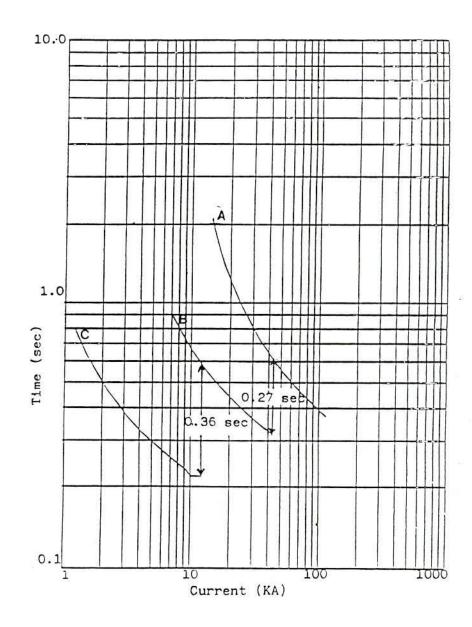


Figure 2.5: Time-current characteristics of relays A, B and C with the presence of a 10 MVA cogenerator and keeping all relay settings as in Fig. 2.4 (on 3.3 kV base).

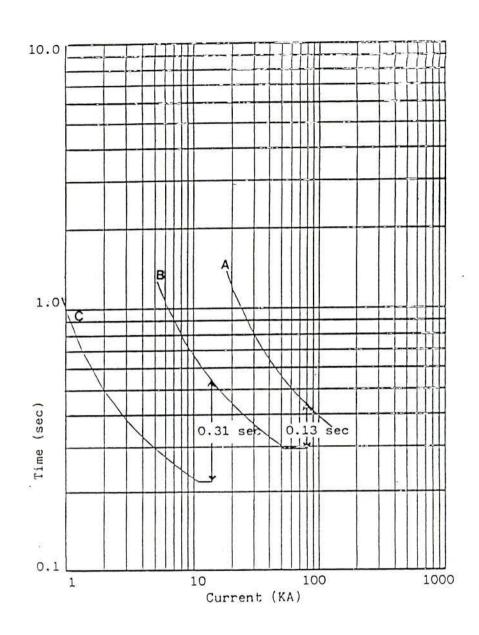


Figure 2.6: Time-current characteristics of relays A, B and C with the presence of a 40 MVA cogenerator and keeping all relay settings as in Fig. 2.4 (on 3.3 kV base).

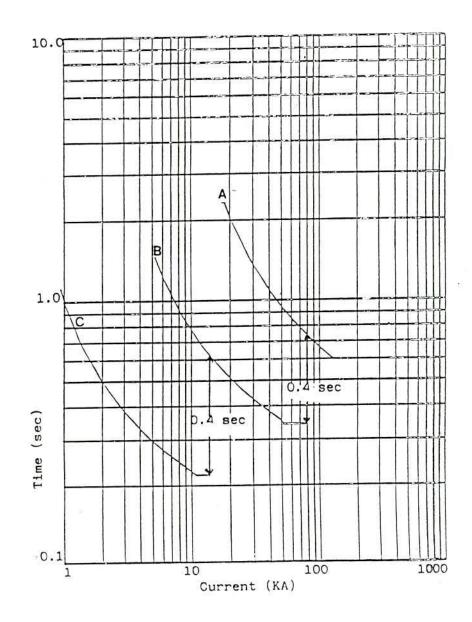


Figure 2.7: Time-current characteristics of relays A, B and C as in Fig. 2.6, but with modified settings to achieve proper discrimination (on 3.3 kV base).



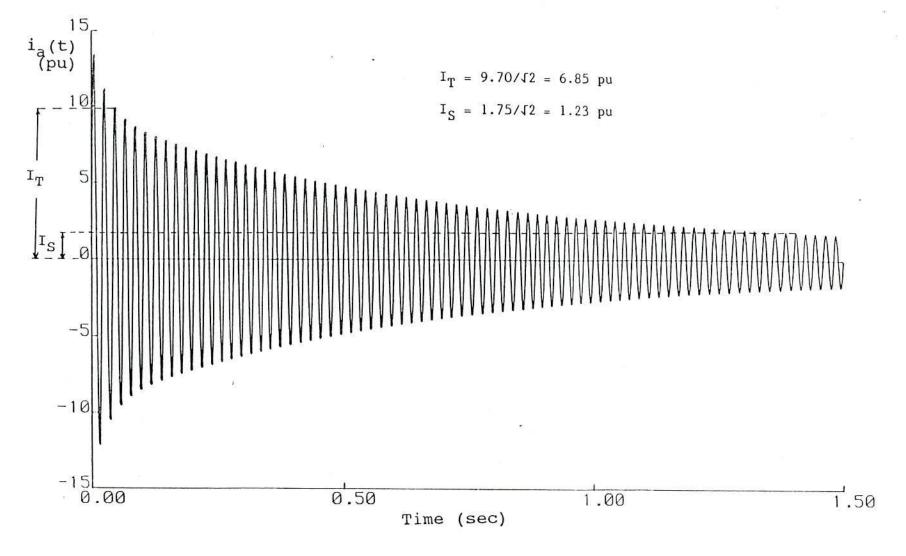


Figure 2.8: Phase "a" current for a three phase fault at the generator terminals.

CHAPTER THREE

DIGITAL RELAYING

3.1. <u>Introduction</u>

This chapter presents a survey of digital relaying techniques and forms a background for subsequent description and analysis of the new protection concept which is the central theme of this project. Power systems are growing very fast and getting more and more complex. Consequently, power supply authorities and educational institutions have undertaken extensive research to automate and simplify the operation of such complex systems. In order to achieve this, power system control equipment and protective relay equipment have been given a vital role in maintaining the system's integrity. Such equipments, therefore, must provide more advanced functions with greater reliability and reduce the operator's workload [49]. Rapid development of digital computers has facilitated this task.

The electric supply industry has been one of the earliest and most dedicated users of large digital computers for power system analysis [50]. Small process control computers are a relatively new development, having smaller operating systems than mainframes. These computers are designed to meet specific applications. They are widely used in electric supply industries to perform complex functions such as supervisory control and data acquisition, generation control, economic dispatch etc.. Modern process control computers are microcomputers, which are less costly and smaller in size than the earli-

er versions called mini-computers.

Protection of power system equipment, particularly EHV transmission lines, using mini computers was first considered by Rockefeller [51] in the late 1960's. Rockfeller's first remarkable contribution along with later work [52-55] created a new horizon in this field. Since then a number of analytical papers [56-58] on the protection of transmission lines by digital computers have been published. The performance of a digital relay was much better than its conventional counterpart. The possibility of integrating a digital relay into the hierarchal computer system within the substation was another attractive feature. However, with the advent of the microprocessor it was perceived that a single computer for the protection of all the equipment in a substation with redundancy provided through duplication is not a viable concept [50]. Introduction of the microprocessor is major breakthrough in digital protection. The microprocessor has made it possible to design digital relaying schemes at low cost. Currently available microprocessors can perform all the functions of the 1970's mini-computers at relatively low cost [59,60]. As a result, for the last few years considerable attention has been given to the development of the microprocessor-based digital protection schemes. Different ideas on microprocessor-based algorithms for the protection of transformers, generators, transmission lines and busbars have been published [61-69].

The first step in computer relaying is to derive current and voltage signals from the power system through current and potential transformers, the functions of which are to reproduce the high level

primary analog signals to much lower level analog signals in the secondary circuit. These signals are reduced further to an acceptable computer input level. These very low level analog signals are then sampled and digitised by analog to digital converter. According to the application of some digital relays, the analog signals are filtered by low-pass filters before digitising. The digitised data is then entered into the computer memory and maintained in a scratch pad random access memory. All the noise present in the power system signals under normal and short circuit conditions will, of course, appear in the sampled data entering into the scratch pad random access memory [50]. A/D conversion may contribute to this as well. These distorted digitised signals are then filtered digitally to extract the fundamental components. Finally, these components are used to develop the relay logic program which defines the function of a relay.

3.2. Advantages of digital protection

Although digital relaying is a new concept, it has become an inspiring subject for a large number of researchers worldwide. Most of the major power supply equirent manufacturers in developed countries are actively involved in research on this field. The advantages of digital relaying over its conventional counterpart are the main reasons for putting so much effort into its development. The important advantages are described here.

3.2.1 Low cost

With the dramatic advancement in microchips and their mass production, the cost of digital hardware has been decreasing steadily since the 1970's. Conventional relaying, on the other hand, has become more expensive in the same period. As a consequence, digital relaying is becoming attractive as an economically viable alternative to the conventional system [70]. Since a digital relay is a programmable device, it can successfully perform different functions, defined by the related logic program, simultaneously. This makes digital relaying more economic.

3.2.2 Reliability

Most of the time a conventional relay, solid state or electromechanical, used for the protection of power system equipment, remains idle. So, there is always a probability of failure of its operation at the time of necessity. On the other hand, a digital relay is continuously active. Consequently, a very high degree of self-diagnosis is going on continuously [50]. Many of its peripherials can be used for measuring and monitoring purpose which provide additional diagnosis features. Due to its self-diagnosis capability, a digital relay can detect accidental failure immediately and take corrective actions. These facilities considerably improve reliability.

3.2.3 <u>Flexibility</u>

A digital relay can provide increased versatility, flexibility and sophistication in operation because of its programmability. Modifications or revisions, which are required to change the function of the relay, can be carried out easily by different pre-programmed memory modules [50]. It is possible to develop a common hardware system to serve several relays, each of which has an individual pre-programmed module. This obviously reduces the volume of repair and maintenance work. Alternate input paths can be provided to the relay from the real system. These alternate paths are generally idle and become active when a fault appears in the normal input paths. These alternate paths for data input increase the flexibility and consequently enhance the reliability of the relay.

3.2.4 Performance

There was doubt about the accuracy of the performance of digital relaying in the early days of its development, because sampling of input signals, required for the digital devices, reduces the amount of information contained in the input signals [71]. However, the concept of computer application in the field of power system protection facilitated the study of signal detection, processing and comparison. Application of digital devices eliminates all the physical limitations inherent in the design of conventional relays, such as narrow range of signal processing and hardware complexity for multiplication and division. It is generally expected that the

performance of a digital relay will be equal to that of its conventional counterpart. Latest research and field tests [72-74] have claimed that the performance of digital relays is faster and more accurate than conventional one for the protection of EHV and UHV transmission lines. However, there has always been a dilema in selecting speed and accuracy in digital relaying. High speed relaying has many advantages; primarily, it increases the chance of maintaining the stability of the system by rapid clearing of severe faults. Secondly, it reduces the risk of insulator damage. Thirdly, it minimizes the likelyhood of imposing CT saturation effects on the protective scheme. However, the advantages of high speed may be achieved at the expense of accuracy of relay performance i.e. security of the system. So, in choosing an acceptable trade-off between speed and accuracy, there should be a clear picture as to how far one can sacrifice accuracy for speed.

3.2.5 Additional features

A digital relaying system has a natural but very special feature, the memory action, which provides the scheme with a facility to furnish off-line study and analysis of power system events. Specially designed devices are required to achieve this advantage with conventional schemes. Computation of distance between the relay location and a fault, which is useful information for the maintenance personnel in the case of a permanent fault on a transmission line, is another example of a special feature of digital relaying. Furthermore, digital relaying system presents a distinct advantage

in that the input hardware and signal conditioning places a lower burden on the transducers in comparison with an electromechanical relay. As a result, the cost and size of transducers for digital schemes are less than for electromechanical relay schemes.

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3.3. <u>Digital relaying algorithm</u>

In conventional protective schemes the hardware of the relay is designed to represent its operating characteristics. So, an overcurrent relay, for example, cannot be used for overvoltage protection. A computer-based relay, on the other hand, has flexible hardware. It can perform functions, like monitoring, measuring of power system signals and supervisory control of power system equipment. It can also be used as a specific protective device. It is the application software which makes the hardware perform according to the user's desire. The software i.e. mathematical expressions in special language, which is used to filter the digitized raw data and define the relay operation logic, is called the relay algorithm. Many algorithms viz. sample and first derivative [52], first and second derivative [54], curve fitting [75], full cycle Fourier method [76], Fourier method with shortened window [70], Walsh function method [77], least squares fitting [78] and differential equation based method [79] have been published particularly for the protection of transmission lines. It has been revealed from literature survey that amongst all algorithms full-cycle Fourier method is the most suitable one in choosing an acceptable compromise between speed and accuracy of response of the algorithm. This had made the

Full-cycle Fourier algorithm the rational choice for developing the microprocessor based technique of this research work. Thus only this algorithm is discussed here.

3.3.1 <u>Full-cycle Fourier algorithm</u>

The full-cycle Fourier algorithm was proposed first by Ramamoorty [76] as an approach to transmission line protection. In this algorithm, power system signals, containing dc offset transients and harmonics, are sampled over one cycle of the fundamental frequency. Assuming the input waveform over this period to be repetitive, Fourier analysis techniques can be applied to extract the fundamental components of the input waveforms i.e. voltage and/or current. These are then used to develop the protection logic. D.C. offset and other harmonics will not have much effect on these values. Accuracy can be improved by increasing sampling rate. The fundamental component is computed using a fixed number of samples. Thus when the computer reads into its memory the newly arrived sample, the first sample in the previous ensemble is deleted, and a fresh calculation is made on the new set. Since a digital computer must spend some time in acquiring the samples and for each set of computation, the sampling rate should be chosen according to the processor capability.

The mathematical theory can be explained by considering a current input signal i(t), which is periodic. The general Fourier formula of the function is

$$i(t) = a_0/2 + a_1 \cos(\omega t) + a_2 \cos(2\omega t) + \dots + b_1 \sin(\omega t) + b_2 \sin(2\omega t) + \dots$$
 (3.1)

Or,

$$i(t) = a_0/2 + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)]$$
 (3.2)

where,

$$a_{n} = \frac{1}{\pi} \int_{0}^{2\pi} i(t) \cos(n\omega t) d\omega t \qquad (3.3)$$

$$b_{n} = -\frac{1}{\pi} \int_{0}^{2\pi} i(t) \sin(n\omega t) d\omega t$$
 (3.4)

By using eqns. (3.3) and (3.4) the required fundamental and/or any harmonic component can be extracted from a power system signal. Let $\Delta\omega$ t be the sampling interval in radians. This gives $N=2\pi/\Delta\omega$ t the number of samples per cycle of fundamental component. The integrals in eqns. (3.3) and (3.4), which is required for determination of the fundamental component, can be found using the trapezoidal rule as follows:

$$a_1 = \frac{1}{N} [i_0 + 2i_1 \cos(\Delta \omega t) + 2i_2 \cos(2\Delta \omega t) + \dots + i_N \cos(N\Delta \omega t)]$$
(3.5)

$$b_{1} = \frac{1}{N} \left[2i_{1} \sin(\Delta \omega t) + 2i_{2} \sin(2\Delta \omega t) + \dots + 2i_{N-1} \sin((N-1)\Delta \omega t) \right]$$
(3.6)

where i_0 , i_1 , i_2 i_N are sample values of the input current at $\Delta \omega t$ intervals. The cosine and sine components of the fundamental can also be expressed at sample point k as follows:

$$a_1^{(k)} = - [i_{k-N} + i_k + 2 \sum_{\ell=1}^{N-1} i_{k-N+\ell} \cos(\frac{2\pi \ell}{N})]$$
 (3.7)

$$b_{1}^{(k)} = - \left[2 \sum_{\ell=1}^{N-1} i_{k-N+\ell} \sin(\frac{2\pi \ell}{N}) \right]$$
(3.8)

Similarly, it is possible to evaluate cosine and sine parts of voltage fundamental component. The time domain representation of current fundamental component ($I_{f.c.}$) can be obtained from its rectangular components a_1 and b_1 as follows:

$$I_{f.c.}(t) = J(a_1^2 + b_1^2) \sin(\omega t + \tan^{-1}(a_1/b_1))$$
 (3.9)

or,

$$I_{f.c.}(t) = J(a_1^2 + b_1^2) \cos(\omega t + \tan^{-1}(-b_1/a_1))$$
 (3.10)

where ω is the fundamental angular frequency.

The algorithm responds accurately, smoothly and slowly as the samples of highly distorted fault waveform enter gradually into the data window. A comparative study has been presented in ref [50], which shows that the filtering performance of this algorithm is the best amongst all algorithms using the same window length. It can be used with a data window of multiple cycles for sharper filtering but the response will be slower.

3.4. Conclusion

In digital relaying there is no single algorithm which is universally optimum. The processor capability, filtering performance, relay-

ing speed and accuracy, which are to some extent conflicting requirements, are the main factors to be considered in choosing an algorithm for a digital protection scheme.

It has been shown in ref [50] that algorithms with short data window lengths like, sample and first derivative, first and second derivative, Fourier algorithm with shortened window etc., are fast, but the results are always prone to errors due to the presence of higher harmonics in the power system signals. On the other hand, in the case of the full-cycle Fourier algorithm the results do not stabilize near the expected values until the full one cycle (12 samples or 16 samples) data window moves into the postfault interval. However, the algorithm results in a slow, smooth and accurate response to badly distorted fault signals. A tripping decision can be safely made by performing trip above threshold check for two samples in many applications. If the post fault steady-state magnitude is well above the threshold, the computed values will cross the decision threshold well before the window is filled with post fault data. The smooth response pattern assures that the results will not swing back outside the threshold as might happen with short-window algorithm. So, it is possible to initiate a fault trip decision in much less than one cycle in these cases. These advantages of the full-cycle Fourier algorithm have made it a popular choice for digital relaying.

CHAPTER FOUR

DEVELOPMENT OF A DIGITAL PROTECTION SCHEME

4.1 <u>Introduction</u>

It has previously been stated that the parallel operation of an industrial cogeneration plant with a utility system is beneficial to the industrial customer, in particular, because it reduces the overall expenditure on energy, and increases the operational flexibility and supply security of the industrial plant. These benefits are gained at the expense of a more sophisticated protection scheme for the interconnected system, particularly when the interface link is intended to carry power in both directions under normal operating conditions. An industrial plant with a considerable cogeneration capacity will be expected to continue supplying a part of its production, independently, in the event of a fault on the utility or on the interface link. If, however, a fault occurs on the industrial busbar, to which both the utility and cogenerator are connected, there is no alternative but to shut down the whole industrial plant. Therefore, in order to provide the operational flexibility and supply security to the industrial plant, the protection scheme must be capable, initially, of locating a fault on the interconnected system, and then taking action according to the fault location, i.e. either allow the plant to run independently or shut down the whole industrial plant. This requirement adds to the cost and complexity of a protection scheme if conventional protection technology is used. Thus, a simple, cheap but reliable protection scheme, which

could perform the same function as the complex and expensive conventional scheme, would be highly desirable.

With a view to meeting the aforesaid requirements, a new microprocessor based technique has been developed which would be capable of detecting as well as locating symmetrical or unsymmetrical short circuit faults anywhere on a utility interconnected industrial system having cogeneration facilities. After detection and location, the type of the fault can also be determined by the microprocessor based protection scheme.

4.2 <u>Proposed technique for fault detection and location</u>

4.2.1 <u>Basic principle</u>

The proposed technique is based on detecting the direction of positive phase sequence (pps) currents [80]. This may be best illustrated by reference to Fig. 4.1 and 4.2, both of which represent a utility interconnected industrial cogeneration system having two different operating conditions prior to faults. The pps current will be referred to only as "current" hereafter.

Figs. 4.1(a), 4.1(b), 4.1(c) and 4.1(d) show the directions of current flow at four selected positions 1, 2, 3 and 4 under both normal operating conditions and short circuit faults on the utility side (beyond position 4), the link (between positions 3 and 4), the industrial busbar and the generator circuit (between position 1 and the generator terminals) respectively. It is assumed that the indus-

trial system is importing power from the utility (i.e. industrial generation is less than the motor load) during the normal operating condition. It is evident that a fault causes the direction of currents to change at one or more positions depending on its location.

Figs. 4.2(a), 4.2(b), 4.2(c) and 4.2(d) also show the directions of current flow at the same positions under normal operating conditions and short circuit faults at the same locations as mentioned above. In this case, however, it is assumed that the industrial system is exporting power to the utility (i.e. industrial generation is greater than the motor load) during normal operating conditions. It is seen that the faults, in this case, cause the current direction to change in a way, which is different from the previous case.

It is, however, evident from Figs. 4.1 and 4.2 that there is a unique combination of the directions of currents at the selected four positions for each condition, viz. normal operation with power import and power export, fault at the industrial bus, the generator circuit, the link and the utility side. Therefore, a decision on whether a fault has occurred and where it has occurred can be achieved by first detecting the directions of current flow at these positions and then identifying the unique combination of their directions. This forms the basis of the proposed technique.

If the fault occurs in the motor circuit (i.e. between position 2 and the motor terminals), the directions of currents may remain exactly the same as under the normal operating conditions shown in Fig. 4.1. However, the current magnitude at position 2 under this

fault condition will be much higher than that under normal operating conditions. Therefore, this fault could be detected by comparing the current magnitude at position 2 with a chosen threshold.

4.2.2 <u>Detection of pps current direction</u>

The determination of current direction can be described with reference to the normal operating condition of Fig. 4.2. It is assumed that the interconnected industrial system is operating at a lagging power factor with a power factor angle of θ° . The current at position 3, for example, can be expressed by $I \angle \theta^{\circ}$ i.e. I_{real} - $\mathrm{jI}_{\mathrm{img}}$ with respect to a polarising reference voltage, which is the pps voltage at position 3. If, however, the power is imported from the utility, the current direction at this position will be reversed and can be expressed by $I/-\theta$ °±180° i.e. $-I_{real}$ + jI_{img} with respect to the same polarising reference. This suggests that the sign of the imaginary component (IC) of a current can be used as a means to determine the current direction under any conditions, if the same polarising reference is maintained. It is apparent from the above mentioned two current expressions that the sign of the real component (RC) can also be used to determine the current direction. However, it has been observed from fault studies on the simulated system, described in the next chapter, that the sign of the RC of a current does not always change with the reversal of the current direction, whereas, the imaginary component does. For example, while the industrial system is operating with 20 MVA generation and 30 MVA motor load at 0.9 lagging power factor, a line-to-line fault, having

a fault path resistance of 0.3α , is applied at the industrial customer busbar. The prefault and post fault currents at position 2, obtained from load flow and fault analysis, are as follows:

I (prefault) =
$$-0.675 + j \cdot 0.3269 \text{ pu}$$

I (post fault) = $0.32879 - j \cdot 1.071 \text{ pu}$

Whereas, for a single line-to-ground fault, having the same fault path resistance, at the same busbar, the prefault and post fault currents at position 2 are as follows:

The above currents have been calculated on the basis of a chosen reference direction, which is discussed in the following paragraph. From the above example, it is clear that, unlike RC, the IC of a current always changes with the reversal of the current direction. Thus, only the IC is considered as a suitable means to detect the direction of a current.

The directions of currents at positions 1, 2, 3 and 4 are designated (either positive or negative) in the following way for the implementation of the proposed technique. Under normal operating conditions when the generator feeds power to the industrial busbar and the industrial system exports power to the utility, the directions of current flow at different positions are shown in Fig. 4.2. Under this condition, the directions of current flow at positions 1, 3 and 4 are designated as positive reference direction and that at position 2, while the motor consumes power from the industrial bus,

as negative reference direction. Due to these chosen directions, currents at positions 1, 3 and 4 can be expressed by $I\angle\theta^\circ$ i.e. I_{real} - I_{limg} and that at position 2 by $-I\angle\theta^\circ$ i.e. $-I_{real}$ + I_{limg} . These two current expressions, therefore, indicate that the negative sign of the IC (of the first expression) represents the designated positive direction and that of positive sign (of the second expression) represents the negative direction. A fault at the generator circuit, for example, causes the reversal of currents at these positions as shown in Fig. 4.2(d). This results in the changes of signs of ICs of currents at the corresponding positions if the polarising references at those positions remain the same, as is the case here. This is discussed in the following section.

4.2.3 <u>Polarising reference voltage</u>

The direction of flow of an alternating current is not an absolute quantity. It can only be determined with respect to some reference which must also be an alternating quantity. Under normal operating conditions, the pps voltage of the industrial busbar, shown in Fig. 4.1, is chosen as the common reference. This is used as the polarising reference for determining the current directions at positions 1, 2 and 3, since these are electrically very close to the industrial busbar. The polarising reference for position 4 can also be obtained from the same reference but referred to the high voltage side of the interfacing transformer. The phase shift introduced by the vector group of the transformer winding should be taken into account when referring the chosen reference to the high voltage side.

The following observation has been made from fault studies. Under solid and low resistance fault conditions, it has been found that the phase angle of the pps voltage of the industrial busbar slightly deviates from its prefault value (i.e. the chosen reference). For example, when the system is operating with 20 MVA generation and 40 MVA motor load at 0.9 lagging power factor, a single line-to-ground fault at the industrial busbar causes the phase angle of the pps voltage of the industrial busbar (say V_l) to change from its prefault value as follows:

For a solid fault -

$$V_1$$
 (prefault) = 1.0 \angle 0°

$$V_1$$
 (post fault) = 0.87635 / 0.00617°

For the same fault but through an arc resistance of 0.3α -

$$V_1$$
 (prefault) = 1.0 $\angle 0^\circ$

$$V_1$$
 (post fault) = 0.91799 /-3.6°

However, it has been observed from the study that the prefault pps voltage can safely be used as the polarising reference for determining the current direction under both normal and fault conditions.

4.2.4 <u>Induction motor contribution to a short circuit fault</u>

In the above description of the proposed technique, it has been assumed that the current in the motor reverses its direction during system faults, since induction motors contribute current to symmet-

rical or unsymmetrical short circuit faults in the system. A literature survey on motor contribution to a fault is presented in this section to support the assumption made in the description of the technique.

Induction motors are widely used in industry due to their low cost, dependability and versatility. They represent, frequently, a very high percentage of the total connected load in many process industries [81]. When an industrial power system with concentrated induction motor load is short circuited, the fault current contribution from the motors is quite appreciable. This could initially be as high as 25 percent of the total fault current [82]. The contribution by an individual small motor to a phase fault may be negligible but the contribution by a group of small motors or by a large one may become significant and thus may not be ignored [6]. The public electric supply, to which an industrial plant has an interconnection, and the synchronous machines of the plant are the principal sources of contribution to a short circuit in the plant but induction motors also contribute significantly to the total short circuit current.

Unlike synchronous machines, an induction motor has no external field supply but it has a rotor winding, in which an E.M.F. is induced by relative motion of the rotor conductors and the magnetic field produced by the stator current. In order to provide a conducting path for the current in the rotor winding, it is short circuited. A rotor field, which sets up unidirectional torque in interaction with the stator field, is established by the induced rotor

current [83]. The rotor flux is a function of both stator and rotor currents. Under short circuit conditions at the motor terminals, the terminal voltage reduces or collapses and the trapped rotor flux continues to generate a driving voltage in the stator winding. The motor, therefore, acts as a generator and feeds fault current into the short circuit [36]. However, the rotor flux, and thus the fault contribution, decays exponentially and eventually ceases, since there is no field excitation. The decay of the flux is controlled by the ratio of inductance and resistance of the associated flux and current path.

The fault current contribution from induction motors like all other rotating machine sources is likely to be asymmetrical. It consists of a symmetrical ac component and a dc offset, both of which decay exponentially with time. The significant point is that the fault current, contributed by an induction motor decays much faster than that from a synchronous machine since the time constant of the former is generally about one tenth of the latter [84]. However, the contribution from a motor of high power rating or high speed, takes a relatively longer time to decay than that of smaller machines. When an industrial electrical system is short circuited some distance from the motor terminals, the external impedance, between the motor terminals and the system short circuit, reduces the magnitude of the initial contribution but increases the time constants from their respective values under terminal short circuit condition. The motor contribution, therefore, decays more slowly and remains appreciable for several cycles [85].

During a three phase short circuit on an industrial system, induction motors may contribute or may continue to act as motors, depending on their location in the system relative to the fault. Yu et al [86] have shown that motors, connected to the faulted bus or downstream of the faulted bus, contribute to the fault when the voltages of those buses drop or collapse. This contribution remains appreciable for few cycles, but other motors, connected upstream of the faulted bus, still act as motors. Huening [87] has given a detailed procedure for calculation of the fault current contribution by induction motors in an industrial system. He has shown that in a particular example of a three phase short circuit the symmetrical rms value of the fault current contribution by a group of ten motors, each 1250 HP, 4.0 kV, 1800 rpm, decays to about 58.9 percent of its initial peak value (9.12 KA) three cycles after the fault. Huening and Stebbins [88] have also studied the behaviour of motor contribution to a fault on an industrial system, where the main incoming busbar supplies the motors, at a lower voltage level, via a 1000 ft long feeder. This study shows that the rms value of the ac component of the contribution by the motors to a three phase fault at the incoming bus decays to about 15 percent of its initial value after four cycles from the instant of fault. Cooper et al [84] have presented a set of test results, which show the magnitude and the duration of fault current contribution by induction motors of different ratings, varying from 408 KVA, 3.22 kV to 19 MVA, 11kV. It shows clearly that both ac and dc component of the fault contribution are quite appreciable even after four cycles from the fault

inception. It has also been shown [36] that the fault current contribution from an induction motor, 500 HP, 6.6 kV, to a three phase terminal short circuit is about 1.0 PU of its rated current at 100 msec after the fault. The same author shows that the contribution of a 3000 HP, 6.6 kV motor to a single phase terminal fault is about 2.5 PU at the same instant.

It is, therefore, evident from the published literature that a large motor or a group of small motors in an industrial system do contribute fault current to a symmetrical or unsymmetrical short circuit at the motor terminals or remote from them. Although this contribution decays quickly, depending on the size, speed and time constants of the machine, it remains quite appreciable at least up to four cycles from the instant of fault inception. This is quite sufficient time for an algorithm, based on the proposed technique, to detect and locate a fault. In fact, the developed algorithm can detect and locate most faults within one cycle following the fault inception. This will be demonstrated in chapter 6.

4.3 <u>Determination of type of fault</u>

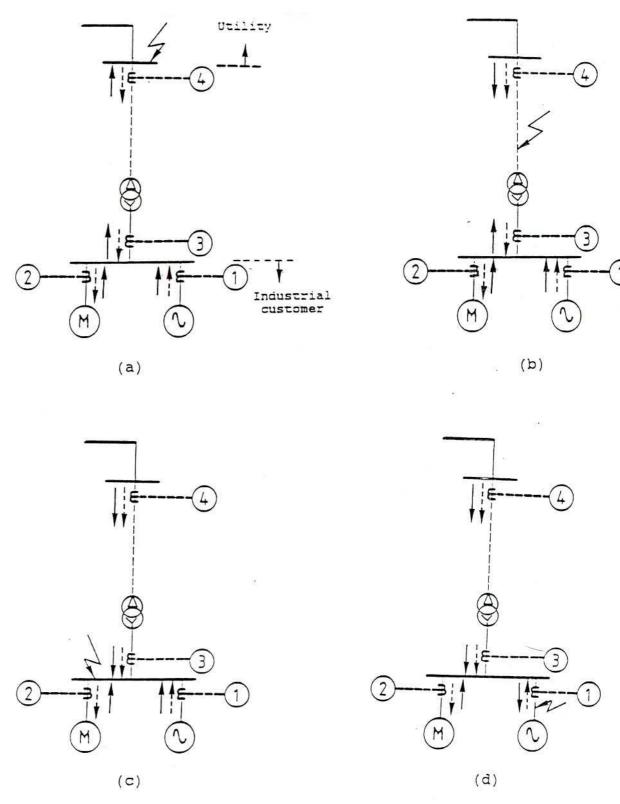
4

After detecting a fault and locating its position using the technique, described earlier, the type of the fault can also be determined from off-line diagnosis of the post-fault phase current data. The fault type classification is based on identifying the phases carrying maximum fault current and checking the presence of zero sequence current. The type of fault can be determined through the following steps.

Firstly, the magnitude of the maximum current amongst the phases a, b and c is evaluated. There could be a case when the magnitude of currents in two phases are equal and greater than the third one (as in the case of a line-to-line fault), or the magnitude of currents in all three phases are equal (as in the case of a three phase fault). In these cases, any one of the values having equal magnitudes is considered as the maximum. The next step is to determine the status of each phase current and zero sequence current as follows. If the ratio of the magnitude of each phase current to the magnitude of the maximum current is greater than a preselected value, C_1 , the status of the corresponding phase is set to "1"; otherwise it is set to "O". Similarly, if the ratio of the magnitude of the zero sequence current to the magnitude of the maximum current is greater than another preselected value, ${\tt C}_{\!2}$, the status of zero sequence current is set to "l"; otherwise it set to "O". The value of C_1 and C_2 have been selected from the results of fault analysis. The procedure for selecting these values will be discussed in the next chapter, where detail description of the simulated system and the fault analysis have been presented. Finally, the types of fault can be identified from the status of all phases and zero sequence currents by applying the criteria, shown in the following table 4.1.

Table 4.1 : Criteria for fault type identification.

	status				
criterion	phase A	phase B	phase C	zero seq.	fault type
1	1	1	1	0	. Three phase
2	1	. 0	. 0	1	. Phase A-to-ground
3	0	1	0	1	. Phase B-to-ground
4	0	0	1	1	Phase C-to-ground
5	1	1	0	0	Phase A-B
6	0	1	1	0	Phase B-C
7	1	0	1	0	Phase A-C
8 .	1	1	0	1	Phase A-B-to-ground
9	0	1	1	1	Phase B-C-to-ground
10	1	0	1	1	Phase A-C-to-ground



---- Normal operating condition

Fault condition

Figure 4.1: Directions of positive phase sequence currents at positions 1, 2, 3 and 4 under normal operation with power being imported to the industrial system and with faults at different locations.

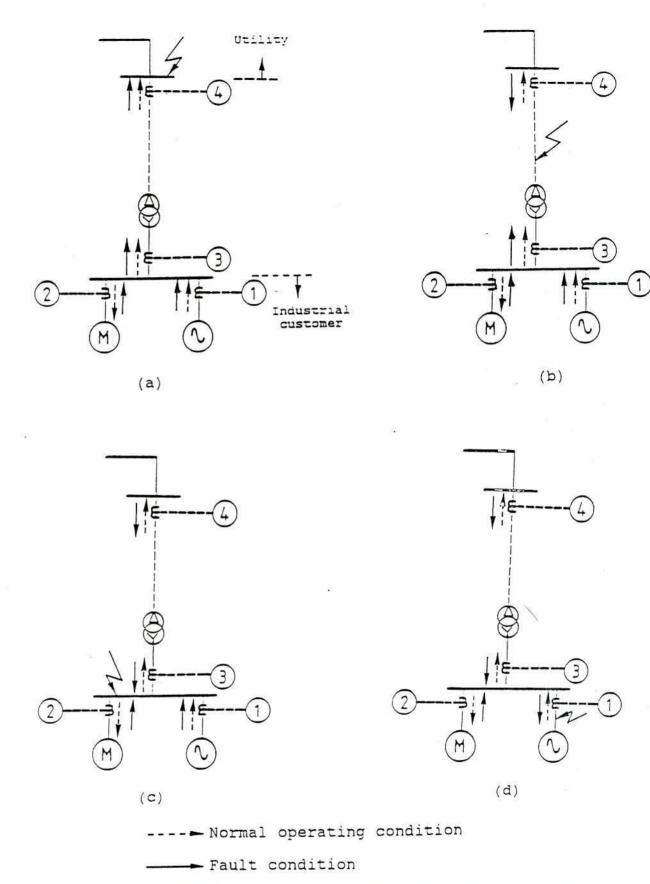


Figure 4.2: Directions of positive phase sequence currents at positions 1, 2, 3 and 4 under normal operation with power being exported to the utility and with faults at different locations.

CHAPTER FIVE

COMPUTER IMPLEMENTATION OF FAULT DETECTION AND LOCATION TECHNIQUE

<u>List of symbols</u>

- H_1 , H_2 and H_3 are the high voltage terminals of a transformer.
- \mathbf{X}_1 , \mathbf{X}_2 and \mathbf{X}_3 are the low voltage terminals of a transformer.
- $\rm V_{A1},~V_{B1}$ and $\rm V_{C1}$ are the positive sequence voltage drops from $\rm H_1,$ $\rm H_2$ and $\rm H_3$ to neutral respectively.
- ${
 m V_{al}},~{
 m V_{bl}}$ and ${
 m V_{cl}}$ are the positive sequence voltage drops from ${
 m X_1},$ ${
 m X_2}$ and ${
 m X_3}$ to neutral respectively.
- I_{A1} , I_{a1} are the positive phase sequence currents on the high and low voltage sides respectively of $a\triangle/Y$ transformer.
- V_{A2} , I_{A2} are the negative phase sequence voltage and current respectively on the high voltage side of a Δ/Y transformer.
- v_{a2} , I_{a2} are the negative phase sequence voltage and current respectively on the low voltage side of a \triangle/Y transformer.
- I is the rms value of a current.
- i is the instantaneous value of a current.
- $i_{\scriptscriptstyle +}$ is the instantaneous value of a positive sequence current.
- $\mathbf{I}_{\text{re}},~\mathbf{I}_{\text{im}}~$ is the real and imaginary part of a fundamental posi tive sequence current.
- i, is the kth sample of a current.
- i_a , i_b , i_c are the instantaneous values of current through phase a, b and c respectively.
- t_k is the time at kth sample.

- T is the time period per cycle of the fundamental frequency.
- θ is the power factor angle.
- E is the rms internal emf of a machine under prefault conditions.
- x_d , x'_d , x''_d are the steady state, transient and subtransient reactances respectively of a machine.
- T'_d , T''_d are the transient and subtransient short circuit time constants respectively of a machine.
- Ta is the armature time constant of a machine.
- δ is the point on the wave at which the fault occurred.

5.1 <u>Introduction</u>

As stated in chapter 1, in order to provide operational flexibility and supply security to an industrial cogeneration system, having an interconnection with a utility, the fault location capability of the protection scheme is an essential requirement. However, a conventional relaying scheme having this capability is complex and thus expensive [6,8,20]. With a view to introducing a simple, cheap and reliable alternative to the conventional scheme, a new technique has been developed to detect as well as locate symmetrical and unsymmetrical short circuit faults anywhere on such an interconnected system. It is intended that the technique is to be implemented on a microprocessor based protective scheme. Both the interconnected industrial cogeneration system and the microprocessor based protection scheme have been simulated on a mainframe computer in order to

test the validity of the new technique. There are four main areas in this simulation as shown in Fig 5.1. This chapter describes the various parts of the simulation.

5.2 <u>Simulation of the utility interconnected cogeneration system</u>

The simulated system used for this study is shown in Fig. 5.2. It is basically an industrial plant, interconnected with a utility. The industrial plant is assumed to consist of a generator with a maximum capacity of 30 MVA and induction motor loads with a maximum demand of 40 MVA. The loads are, however, lumped together as a single motor for convenience. Both the generator and the lumped single induction motor are connected directly to the 11 kV customer busbar, called bus 1, which is interconnected with a 33 kV utility busbar, called bus 3, through an interface link. The link consists of a 500 meter long cable and a 40 MVA, 33kV/11kV, Dyl transformer. The high tension terminals of the transformer are considered as bus 2. The neutrals of both the generator and Y side of the interface transformer are grounded through a reactance of 0.5 α . The utility is represented by a generator, whose neutral is solidly grounded and fault infeed capability is 600 MVA. Under normal operating conditions, the interface link is intended to handle bidirectional power flow, which is simulated by changing the generator capacity and/or the motor load. Currents are monitored at positions 1, 2, 3 and 4 as shown in Fig. 5.2.

5.2.1 Phase shift introduced by the \(\Delta / Y \) transformer

The determination of pps current direction at position 4 of the system under consideration requires a polarising reference. As stated in Chapter 4, this reference can be evaluated from the chosen common reference (i.e pps voltage at bus 1) referred to the delta side of the interface transformer.

 $A \triangle/Y$ connected transformer always introduces phase shifts in currents and voltages between its primary and secondary windings. The amount of the phase shift depends on the vector group to which the transformer windings belong. The most commonly used group in practice are Dyl and Dyll. In the case of Dyl, the transformer windings are such that the positive sequence voltage drops from the high voltage terminals to neutral lead that of the corresponding low voltage terminals to neutral by 30°. In the case of Dyll, however, the formers lag the latters by 30° [89].

In order to reduce the computational burden, a more simple relationship between the phase sequence voltages and currents on the two sides of the transformer, which involve only the use of the j operator, is preferable. This can be achieved by connecting the low voltage terminals of the transformer to the phases of the power line in a particular order with respect to that of the high voltage terminals. This can be illustrated with reference to Figs. 5.3 and 5.4.

Fig. 5.3(a) shows the vector diagram related to group Dyl, where the positive sequence voltage of phase "a" at the high voltage side

 (V_{A1}) leads that at the low voltage side (V_{a1}) by 30°. For this group, the connection configuration of the transformer terminals to the phases of the power line is shown in Fig. 5.3(b). If, however, the low voltage terminal X_3 is connected to phase "a", X_2 to phase "c" and X_1 to phase "b", keeping the high voltage terminals to phase connections unchanged, as shown in Fig. 5.4(a), V_{A1} will lag V_{a1} by 90°. The vector diagram for this connection is shown in Fig. 5.4(b). The positive phase sequence currents on the two sides of the transformer will maintain the same relation as for the case of positive phase sequence voltages. However, the negative phase sequence current and voltage on the high voltage side will lead that at the low voltage side by 90° [90].

In summary, the relationship between the phase sequence voltages and currents, expressed in per unit values, on the two sides of the transformer, having a connection configuration shown in Fig. 5.4(a), can be given as follows:

$$V_{a1} = j V_{A1},$$
 $I_{a1} = j I_{A1}$ $V_{a2} = -j V_{A2},$ $I_{a2} = -j I_{A2}$ (5.1)

5.3 <u>Generation of current samples</u>

Having chosen the system, the generation of current samples at positions 1, 2, 3 and 4 under both prefault and postfault conditions is the first step of the simulation.

5.3.1 <u>Prefault current samples</u>

Busbar 1 is chosen as the reference bus. Thus the voltage at this bus is considered as $V_1=1.0\sqrt{0}\,^\circ$. Consequently, the polarising reference at position 4 will lag the chosen reference by 90°, as explained in the previous section and in accordance with eqn. (5.1). $I_1\sqrt{\theta_1}$, $I_2\sqrt{\theta_2}$, $I_3\sqrt{\theta_3}$ and $I_4\sqrt{\theta_4}$ are the rms values of currents at positions 1, 2, 3 and 4 respectively, which are obtained from the load flow calculation. The voltages at busbars 2 and 3, and the internal emfs of the machines are also calculated, since they are required at a later stage in the short circuit analysis. It is assumed that the sampling frequency is 600 Hz (i.e. 12 samples per cycle of 50 Hz frequency). The kth sample of phase "a" current, for example, can be expressed as follows:

$$i_{ak} = i_a(t_k) \tag{5.2}$$

Therefore, the current samples at positions 1, 2 and 3 are calculated from the following equations:

$$i_{ak1} = \int_{0}^{2} I_{1} \cos(\omega t_{k} + \theta_{1})$$
 (5.3)

$$i_{ak2} = \int_{2}^{2} I_{2} \cos(\omega t_{k} + \theta_{2})$$
 (5.4)

$$i_{ak3} = \sqrt{12} I_3 \cos(\omega t_k + \theta_3)$$
 (5.5)

The current at position 4 lags those at position 1, 2 and 3 by 90°. This is because of the fact that the polarising reference at position 4 lags that at position 1, 2 or 3 by 90°. Thus, current samples at position 4 are computed from the following equation.

$$i_{ak4} = \sqrt{12} I_4 \cos(\omega t_k + \theta_4 - 90^\circ)$$
 (5.6)

5.3.2 <u>Fault analysis</u>

Before going on to the discussion of the generation of current samples under fault condition, a brief description of the analysis of different types of faults, considered in this work, is presented in this sub-section.

When a fault occurs in a power network, the magnitude of short circuit current is determined by the internal emfs of the machines and the impedance of the fault path. Short circuit faults can be classified as symmetrical and unsymmetrical, both of which may be either direct short circuit or through an impedance. Symmetrical faults involve all three phases. Most of the faults that occur on power systems are , however, unsymmetrical faults, which include single line-to-ground, line-to-line and double line-to-ground. There are various methods for fault analysis [91,92]. The method used here is based on the bus frame of reference and bus impedance matrix. The first step of this method is to determine the prefault bus voltages which are used as initial conditions for fault calculation routine. The bus admittance matrix, Y bus, of the system is then formed from a knowledge of the individual branch impedances. Then, the bus impedance matrix, \mathbf{Z}_{bus} , is obtained by inverting the \mathbf{Y}_{bus} . Finally, the total fault current, postfault voltages at different busbars and postfault currents in different branches are computed. The flow diagram of the fault analysis algorithm [92] is shown in Fig. 5.5.

5.3.2.1 <u>Symmetrical faults</u>

The formulae developed here are used for the computation of post fault bus voltages and all branch currents under three phase fault condition. The method for developing the formulae is presented with reference to a general n-bus system [92]. However, a simple three-bus system, shown in Fig 5.6, is considered first in order to simplify the analysis. Then the method will be generalised to include n-bus system. The equivalent prefault network of the system, shown in Fig. 5.6, in per phase basis is first assembled as shown in Fig 5.7. It is assumed that the system is operating under known generating and loading condition prior to a fault. From the load flow analysis, the prefault bus voltages are then determined and can be expressed as the three element-vector

$$\mathbf{v}^{0}_{\text{bus}} = \begin{bmatrix} \mathbf{v}^{0}_{1} \\ \mathbf{v}^{0}_{2} \\ \mathbf{v}^{0}_{3} \end{bmatrix}$$
 (5.7)

It is assumed that a short circuit is applied at bus 3. The effect of the short circuit is equivalent to that of connecting a branch of impedance \mathbf{Z}^f between bus 3 and ground. If the short circuit is solid, the fault impedance \mathbf{Z}^f equals zero. The venin's theorem states that the changes in the bus voltages caused by the added branch are equivalent to those caused by the added emf (i.e. prefault voltage of bus 3) with all other sources short circuited as shown in Fig 5.8. According to this theorem, the post fault bus voltages can be

obtained by superposition of the prefault bus voltages and changes in the bus voltages caused by the equivalent emf connected to the faulted bus as shown in Fig. 5.8. This can be expressed by the following vector equation:

$$v^{f}_{bus} = v^{0}_{bus} + v_{T}$$
 (5.8)

 ${v^0}_{\mathrm{bus}}$ is the prefault bus voltage vector defined by eqn. (5.7). The post fault bus voltage vector is defined by

$$\mathbf{v^f}_{\text{bus}} = \begin{bmatrix} \mathbf{v^f}_1 \\ \mathbf{v^f}_2 \\ \mathbf{v^f}_3 \end{bmatrix} \tag{5.9}$$

Finally the third vector, \mathbf{V}_{T} , is referred to Thevenin's bus voltage vector and can be defined by

$$\mathbf{v}_{\mathrm{T}} = \begin{bmatrix} \triangle \, \mathbf{v}_{1} \\ \triangle \, \mathbf{v}_{2} \\ \triangle \, \mathbf{v}_{3} \end{bmatrix} \tag{5.10}$$

where $\Delta\,{\rm V}_1,~\Delta\,{\rm V}_2$ and $\Delta\,{\rm V}_3$ are the changes of voltages at bus 1, 2 and 3 respectively.

It may also be considered here that the changes in the three bus voltages are resulted from the fault current \mathbf{I}^f being drawn from bus (or the current $-\mathbf{I}^f$ being injected into bus 3). Therefore, the fault current vector is defined by

$$\mathbf{I}^{f} = \begin{bmatrix} 0 \\ 0 \\ -\mathbf{I}^{f} \end{bmatrix} \tag{5.11}$$

From nodal analysis, \mathbf{V}_{T} can be expressed in terms of fault current

vector as follows

$$\mathbf{I}^f = \mathbf{Y}_{bus} \ \mathbf{V}_T$$
 or
$$\mathbf{V}_T = \mathbf{Y}^{-1}_{bus} \ \mathbf{I}^f = \mathbf{Z}_{bus} \ \mathbf{I}^f \tag{5.12}$$

where \mathbf{Z}_{bus} is the nodal bus impedance matrix for the network of Fig. 5.7 and can be expressed by

$$\mathbf{z}_{\text{bus}} = \begin{bmatrix} z_{11} & z_{12} & z_{13} \\ z_{21} & z_{22} & z_{23} \\ z_{31} & z_{32} & z_{33} \end{bmatrix}$$
 (5.13)

By substituting eqn. (5.12) into (5.8), we get

$$\mathbf{v^f}_{bus} = \mathbf{v^0}_{bus} + \mathbf{z}_{bus} \mathbf{I^f} \tag{5.14}$$

Before proceeding further, it may be observed that, although the eqn. (5.14) has been derived with reference to a three bus system, it is applicable equally well to a general n-bus system. So, a general case will be considered henceforth. In order to make the eqn. (5.14) applicable to a general case, the short circuit is moved from bus 3 to the general bus q. In this general case, the fault current vector becomes

$$I^{f} = \begin{bmatrix} 0 \\ \cdot \\ -I^{f} \\ \cdot \\ 0 \end{bmatrix} \longrightarrow qth component$$
 (5.15)

Under this general case , when eqn. (5.14) is expanded, it can be

expressed in component form as follows :

$$V^{f}_{1} = V^{0}_{1} - z_{1q} I^{f}$$
......

 $V^{f}_{q} = V^{0}_{q} - z_{qq} I^{f}$
.....

 $V^{f}_{n} = V^{0}_{n} - z_{nq} I^{f}$
(5.16)

The fault current, I^f , is not yet known. However, $V^f_{\ q}$, the postfault voltage of the faulted bus, is related to the fault current as follows:

$$V_{q}^{f} = Z^{f} I^{f}$$
 (5.17)

where $\mathbf{Z}^{\mathbf{f}}$ is the fault impedance.

By substituting eqn. (5.17) into the qth eqn. (5.16), the following expression for the fault current is obtained.

$$I^{f} = \frac{V^{0}_{q}}{Z^{f} + Z_{qq}}$$
 (5.18)

By substituting eqn. (5.18) into (5.16), the following final formulae for the postfault bus voltages are obtained.

$$V_{i}^{f} = V_{i}^{0} - \frac{z_{iq}}{z_{f} + z_{qq}} V_{q}^{0}$$
 for $i \neq q$

$$V_{q}^{f} = \frac{z_{f}}{z_{f} + z_{qq}} V_{q}^{0}$$
(5.19)

If the short circuit is solid, i.e. $Z^f = 0$, eqns. (5.18) and (5.19) are reduced to following form :

$$I^{f} = \frac{V^{0}_{q}}{z_{qq}}$$

$$V^{f}_{q} = 0$$
(5.20)

$$V_{i}^{f} = V_{i}^{0} - \frac{z_{iq}}{z_{qq}} V_{q}^{0}$$
 for $i \neq q$

Having determined postfault bus voltages, postfault currents in all branches can also be evaluated. For example, the fault current, $\mathbf{I_{st}^f}$, in a line which connects buses s and t and has an impedance $\mathbf{Z_{st}}$ can be computed as follows:

$$I_{st}^f = \frac{v_{s}^f - v_{t}^f}{z_{st}}$$
 (5.21)

As stated in section 4.2.4 of Chapter 4, the contribution by a generator or an induction motor to a fault current due to a short circuit is likely to be asymmetrical. It consists of a symmetrical ac component and a dc offset, both of which decay exponentially with time. In order to incorporate these decaying components in fault current, phase "a" instantaneous currents contributed by a generator and an induction motor can be expressed by the following equations (5.22) and (5.23) respectively [85,93]. Due to phase symmetry, fault currents in phase "b" and "c" can easily be obtained.

$$i_a(t) = \sqrt{2(E-V^f_1)} \left[\frac{1}{x^d} + (\frac{1}{x^d} - \frac{1}{x^d}) e^{-t/T'd} + (\frac{1}{x^{"d}} - \frac{1}{x^{"d}}) e^{-t/T"d} \right] \cos(\omega_0 t + \delta)$$

$$-\frac{\sqrt{2(E-V^f_1)}}{x''_d}\cos\delta e^{-t/Ta}$$
 (5.22)

$$i_a(t) = \frac{\sqrt{32(E-V^f_1)}}{x''_d} e^{-t/T''d} \cos(\omega_0 t + \delta) - \frac{\sqrt{32(E-V^f_1)}}{x''_d} \cos\delta e^{-t/Ta}$$
where the postfault bus 1 voltage, (5.23)

$$V_1^f = 0$$
, for a solid fault at bus 1
 $\neq 0$, for a fault through impedance

5.3.2.2 <u>Unsymmetrical faults</u>

Under balanced loading or three phase symmetrical fault condition, the load or fault impedances are assumed to be the same on all three phases; and the voltages, emfs and currents are characterised by three phase symmetry i.e. they are of equal magnitude in each phase but displaced by 120° and 240° in time. So, the system is studied on a per phase basis. Because a knowledge of the voltage and current of one phase can be used to find the corresponding variables on the other two phases. However, in the case of an unsymmetrical fault, neither the voltage nor the current possesses three phase symmetry. It is, therefore, no longer possible to limit the analysis to one phase. In order to reduce the complexity of the analysis, unsymmetrical faults are usually studied by using the method of symmetrical components. The general formulae [92], which have been used for the computation of postfault bus voltages and all branch currents under all types of unsymmetrical faults, are presented in this section.

In unsymmetrical fault cases, the prefault and postfault variables are distinguished by the following symbols

- a) Prefault conditions are indicated by the superscript 0.
- b) Postfault conditions are indicated by the superscript f.
- c) Positive, negative and zero sequence components are indicated by the subscripts +, - and O respectively or collectively by the subscript s.
- d) A number subscript refers to bus coding.

For a balanced n-bus network study the end result of the network model construction is the n*n bus admittance matrix $Y_{\rm bus}$, or its inverse, the bus impedance matrix, $Z_{\rm bus}$. For an unbalanced network study the model gets more complex. This is because of the fact that separate network models are required for three separate symmetrical component (SC) systems (i.e. positive, negative and zero sequence network). Consequently, each element of the n*n admittance (or impedance) matrix of the balance n-bus sy 2m will be required to represent by its SC 3*3 matrix. So, the SC bus admittance (or impedance) matrix of an unbalance n-bus system becomes 3n*3n matrix. This is illustrated by eqn. (5.29). The SC voltage vector of bus 1 (for example) is given by

$$\mathbf{V}_{s1} = \begin{bmatrix} \mathbf{V}_{+1} \\ \mathbf{V}_{-1} \\ \mathbf{V}_{01} \end{bmatrix} \tag{5.24}$$

Therefore, the SC bus voltage vector of a n-bus system is

$$V_{s,bus} = \begin{bmatrix} v_{+1} \\ v_{-1} \\ v_{01} \\ \vdots \\ v_{+q} \\ v_{-q} \\ v_{0q} \\ \vdots \\ v_{sq} \\ \vdots \\ v_{sn} \end{bmatrix}$$

$$V_{s,bus} = \begin{bmatrix} v_{s1} \\ \vdots \\ v_{sq} \\ \vdots \\ v_{sn} \end{bmatrix}$$

$$V_{+n} \\ V_{-n} \\ V_{0n} \end{bmatrix}$$

$$V_{h} = \begin{bmatrix} v_{s1} \\ \vdots \\ v_{sq} \\ \vdots \\ v_{sn} \end{bmatrix}$$

$$V_{+n} = \begin{bmatrix} v_{s1} \\ \vdots \\ v_{sq} \\ \vdots \\ v_{sn} \end{bmatrix}$$

Similarly, the SC bus current vector of the n-bus system is

$$I_{s,bus} = \begin{bmatrix} I_{+1} \\ I_{-1} \\ I_{01} \\ \vdots \\ I_{+q} \\ I_{-q} \\ I_{0q} \\ \vdots \\ I_{sn} \end{bmatrix}$$

$$I_{s,bus} = \begin{bmatrix} I_{s1} \\ \vdots \\ I_{sq} \\ \vdots \\ I_{sn} \end{bmatrix}$$

$$I_{+n}$$

$$I_{-n}$$

$$I_{0n}$$

In order to derive a general formulae for the SC bus voltage vector of n-bus system for unsymmetrical faults, the SC transformation method is combined with Thevenin's method as used in the case of three phase fault situation. In doing this, the eqn. (5.14), therefore, becomes

$$\mathbf{v}^{\mathrm{f}}_{\mathrm{s,bus}} = \mathbf{v}^{\mathrm{0}}_{\mathrm{s,bus}} + \mathbf{z}_{\mathrm{s,bus}} \mathbf{I}^{\mathrm{f}}_{\mathrm{s,bus}}$$
 (5.27)

 $v^f_{s,bus}$ and $v^0_{s,bus}$ are the postfault and prefault SC bus voltage vectors respectively. $v^f_{s,bus}$ is the SC fault current vector representing the SC of fault currents injected at various buses. The fault is again assumed at bus q. So the injected current at bus q equals to v^f_{sq} . So the fault current vector becomes

$$I_{s,bus}^{f} = \begin{bmatrix} 0 \\ \cdot \\ -I_{sq} \\ \cdot \\ \cdot \\ 0 \end{bmatrix} \longrightarrow qth component$$
 (5.28)

Finally the SC bus impedance matrix is defined by

At this point, it is important to note that prefault voltages are, of course, balanced. Therefore, a prefault SC bus voltage vector, ${\bf v}^0_{\rm s,bus}$, contains no negative and zero sequence components, i.e.

$$\mathbf{v}^{0}_{\text{si}} = \begin{bmatrix} \mathbf{v}^{0}_{+i} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} = \begin{bmatrix} \mathbf{v}^{0}_{i} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \qquad i = 1, 2, 3, \dots, n$$
 (5.30)

Having defined the related vectors and matrix, the general formulae for postfault SC bus voltage and fault current vectors for all kinds

of unsymmetrical faults are obtained by solving eqn. (5.27). These are presented in the rest of this subsection. The detailed derivation of these formulae are presented in Appendix I. The following eqns. (5.31) to (5.36) and (5.39) to (5.50) correspond to eqns. (A.17) to (A.22) and (A.23) to (A.36) respectively of Appendix I.

Single line-to-ground fault

The SC voltage vector of the faulted bus q,

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{1 + (\mathbf{Y}^{f}/3)(z_{+qq}^{+z} - qq^{+z}0qq)} \begin{bmatrix} 1 + (\mathbf{Y}^{f}/3)(z_{-qq}^{+z} - qq^{+z}0qq) \\ -z_{-qq}\mathbf{Y}^{f}/3 \\ -z_{0qq}\mathbf{Y}^{f}/3 \end{bmatrix}$$
(5.31)

The short circuit SC current at the faulted bus q,

$$I_{sq}^{f} = \frac{V_{q}^{0}(Y^{f}/3)}{1+(Y^{f}/3)(z_{+qq}+z_{-qq}+z_{0qq})} \begin{bmatrix} 1\\1\\1 \end{bmatrix}$$
 (5.32)

The postfault SC voltage vectors at the buses other than the faulted one,

$$\mathbf{v^f}_{si} = \begin{bmatrix} v^0_i \\ 0 \\ 0 \end{bmatrix} - \frac{v^0_q(Y^f/3)}{1 + (Y^f/3)(z_{+qq} + z_{-qq} + z_{0qq})} \begin{bmatrix} z_{+iq} \\ z_{-iq} \\ z_{0iq} \end{bmatrix} \quad i \neq q \quad (5.33)$$

If the short circuit fault is solid, i.e., $Y^f = \infty$ then the above formulae become as follows :

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{\mathbf{z}_{+qq} + \mathbf{z}_{-qq} + \mathbf{z}_{0qq}} \begin{bmatrix} \mathbf{z}_{-qq} + \mathbf{z}_{0qq} \\ -\mathbf{z}_{-qq} \\ -\mathbf{z}_{0qq} \end{bmatrix}$$
(5.34)

$$I_{sq}^{f} = \frac{v_{q}^{0}}{z_{+qq} + z_{-qq} + z_{0qq}} \begin{bmatrix} 1\\1\\1 \end{bmatrix}$$
 (5.35)

$$V_{si}^{f} = \begin{bmatrix} v_{i}^{0} \\ 0 \\ 0 \end{bmatrix} - \frac{v_{q}^{0}}{z_{+qq} + z_{-qq} + z_{0qq}} \begin{bmatrix} z_{+iq} \\ z_{-iq} \\ z_{0iq} \end{bmatrix}$$
 for $i \neq q$ (5.36)

Fault currents in all branches can be calculated from a knowledge of the postfault bus voltages. For example, a line connecting two buses s and t is characterised by the following admittance matrix.

$$\mathbf{Y}_{s,st} = \begin{bmatrix} y_{+} & 0 & 0 \\ 0 & y_{-} & 0 \\ 0 & 0 & y_{0} \end{bmatrix}$$
 (5.37)

The postfault SC current vector, $\mathbf{I}^{\mathbf{f}}_{s,st}$, flowing through the line can be calculated from the following equation :

$$I_{s,st}^{f} = Y_{s,st} (V_{s,s}^{f} - V_{s,t}^{f})$$
 (5.38)

Line-to-line fault

The SC voltage vector of the faulted bus, q

$$v_{sq}^{f} = \frac{v_{q}^{0}}{1 + Y_{qq}^{f}(z_{+qq} + z_{-qq})} \begin{bmatrix} 1 + Y_{z_{-qq}} \\ Y_{z_{-qq}} \\ 0 \end{bmatrix}$$
 (5.39)

The SC current vector at the faulted bus, q

$$I_{sq}^{f} = \frac{v_{q}^{0} Y^{f}}{1 + Y^{f}(z_{+qq} + z_{-qq})} \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix}$$
 (5.40)

The postfault SC voltage vectors at the buses other than the faulted one are

$$\mathbf{v}^{f}_{Si} = \begin{bmatrix} \mathbf{v}^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{\mathbf{v}^{0}_{q}Y^{f}}{1 + Y^{f}(z_{+qq} + z_{-qq})} \begin{bmatrix} z_{+iq} \\ -z_{-iq} \\ 0 \end{bmatrix} i \neq q \qquad (5.41)$$

If the short circuit is solid, i.e. $Y^f = \infty$, then the above formulae become as follows :

$$V^{f}_{sq} = \frac{V^{0}_{q}}{z_{+qq} + z_{-qq}} \begin{bmatrix} z_{-qq} \\ z_{-qq} \\ 0 \end{bmatrix}$$
 (5.42)

$$I_{sq}^{f} = \frac{v_{q}^{0}}{z_{+qq} + z_{-qq}} \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix}$$
 (5.43)

$$\mathbf{v^f}_{si} = \begin{bmatrix} \mathbf{v^0}_i \\ 0 \\ 0 \end{bmatrix} - \frac{\mathbf{v^0}_q}{\mathbf{z_{+qq} + z_{-qq}}} \begin{bmatrix} \mathbf{z_{+iq}} \\ -\mathbf{z_{-iq}} \\ 0 \end{bmatrix} \quad i \neq q$$
 (5.44)

The branch fault SC current vector can be computed using the eqn. (5.38).

Double line-to-ground fault

The SC voltage vector at the faulted bus q,

$$v_{sq}^f =$$

$$\frac{v^{0}_{q}}{1+(4Y^{f}/3)(z_{+qq}^{+z}-qq^{+z}0qq)^{+}(4Y^{f2}/3)(z_{+qq}^{z}-qq^{+z}-qq^{z}0qq^{+z}0qq^{z}+qq)}$$

$$\begin{bmatrix} 1 + (4Y^{f}/3)z_{0qq} + (4Y^{f}/3)z_{-qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \\ (2Y^{f}/3)z_{-qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \\ (2Y^{f}/3)z_{0qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \end{bmatrix}$$
(5.45)

The short circuit SC current vector at the faulted bus q,

$$I_{sq}^f =$$

$$\frac{(2Y^{f}/3)V_{q}^{0}}{1+(4Y^{f}/3)(z_{+qq}+z_{-qq}+z_{0qq})+(4Y^{f2}/3)(z_{+qq}z_{-qq}+z_{0qq}z_{0qq}+z_{0qq}z_{+qq})}$$

$$\begin{bmatrix} 2 + 2Y^{f}z_{0qq} + 2Y^{f}z_{-qq} \\ -1 - 2Y^{f}z_{0qq} \\ -1 - 2Y^{f}z_{-qq} \end{bmatrix}$$
 (5.46)

The postfault SC voltage vectors at the buses other than the faulted

one is given as follows :

$$\mathbf{v^f}_{si} = \begin{bmatrix} \mathbf{v^0}_i \\ 0 \\ 0 \end{bmatrix} -$$

$$\frac{(2Y^{f}/3)V_{q}^{0}}{1+(4Y^{f}/3)(z_{+qq}+z_{-qq}+z_{0qq})+(4Y^{f2}/3)(z_{+qq}z_{-qq}+z_{-qq}z_{0qq}+z_{0qq}z_{+qq})}{z_{+qq}}$$

$$\begin{bmatrix} z_{+iq}(2 + 2Y^{f}(z_{0qq} + z_{-qq})) \\ z_{-iq}(-1 - 2Y^{f}z_{0qq}) \\ z_{0iq}(-1 - 2Y^{f}z_{-qq}) \end{bmatrix}$$
 for $i \neq q$ (5.47)

If the short circuit fault is solid, i.e. $Y^f = \infty$, the eqns. (5.45), (5.46) and (5.47) become as follows:

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{z_{+qq}^{z}_{-qq} + z_{-qq}^{z}_{0qq} + z_{0qq}^{z}_{+qq}} \begin{bmatrix} z_{0qq}^{z}_{-qq} \\ z_{0qq}^{z}_{-qq} \\ z_{0qq}^{z}_{-qq} \end{bmatrix}$$
(5.48)

$$I_{sq}^{f} = \frac{v_{q}^{0}}{z_{+qq}^{z} - qq^{+z} - qq^{z} - qq^{+z} - qq^{z} - qq^{$$

$$\mathbf{v^{f}_{si}} = \begin{bmatrix} v^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{v^{0}_{q}}{z_{+qq}^{z} - qq^{+z} - qq^{z} 0 qq^{+z} 0 qq^{z} + qq} \begin{bmatrix} z_{+iq}(z_{0qq} + z_{-qq}) \\ -z_{-iq}z_{0qq} \\ -z_{0iq}z_{-qq} \end{bmatrix}$$
(5.50)
for $i \neq q$

The branch fault SC current vector can be computed using eqn. (5.38). All the above voltages and currents are sequence components. The actual phase voltages and currents can be obtained by multiplying the sequence voltages and currents with the symmetrical component transformation matrix T,

$$T = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix}$$
 (5.51)

where $a = 1/120^{\circ}$ and $a^2 = 1/240^{\circ}$.

5.3.3 <u>Generation of fault current samples</u>

Once the phase currents I_a^f / θ_a , I_b^f / θ_b and I_c^f / θ_c at the four selected positions are obtained from fault analysis, current samples at positions 1, 2 and 3 can be calculated from the following equations:

$$i_{akp}^{f} = J2 I_{ap}^{f} \cos(\omega t_{k} + \theta_{ap})$$

$$i_{bkp}^{f} = J2 I_{bp}^{f} \cos(\omega t_{k} + \theta_{bp}) \quad \text{for p = 1, 2, 3}$$

$$i_{ckp}^{f} = J2 I_{cp}^{f} \cos(\omega t_{k} + \theta_{cp})$$

For the case of three phase symmetrical faults, samples of phase currents, contributed by the generator and motor, at positions 1 and 2 are computed using the eqns. (5.22) and (5.23) respectively.

Current samples at position 4 are computed from the following equation:

$$i_{ak4}^{f} = J2 I_{a4}^{f} \cos(\omega t_{k} + \theta_{a4} - 90^{\circ})$$

$$i_{bk4}^{f} = J2 I_{b4}^{f} \cos(\omega t_{k} + \theta_{b4} - 90^{\circ})$$

$$i_{ck4}^{f} = J2 I_{c4}^{f} \cos(\omega t_{k} + \theta_{c4} - 90^{\circ})$$
(5.53)

5.4 <u>Positive phase sequence (pps) current</u>

Having calculated current samples over a period of six cycles (three cycles prefault and three cycles postfault) at each of the four selected positions, the next step of the simulation is the computation of the pps currents at each of these positions. The pps current can be computed from current samples of phases a, b and c using either of the following equations [94]:

$$i_{+k} = [i_a(t_k) + i_b(t_k+T/3) + i_c(t_k+2T/3)]/3$$
 (5.54)

$$i_{+k} = [i_a(t_k) + i_b(t_k-2T/3) + i_c(t_k-T/3)]/3$$
 (5.55)

From eqn. (5.54) it is seen that the sequence current is related to the samples of phase currents measured in the future as long as t_k is considered to represent the present. The eqn. (5.55), on the other hand, shows that the sequence current is related to the samples of phase currents measured in the past. However, eqn. (5.55) has been used in the simulation for this study with the idea that in real time application, the microprocessor memory capacity must be

used to store the samples measured in the past.

5.5 <u>Fundamental component of pps current</u>

In general terms, the pps current computed by eqn. (5.55) is a sinusoidal waveform which contains a fundamental frequency of 50 Hz, higher harmonics and a dc offset. The sampled pps current is then used in the third part of the simulation to extract the fundamental component. This is achieved by using the full cycle Fourier filtering method, described in chapter 3. The filtering algorithm produces the fundamental component at positions 1, 2, 3 and 4 in a rectangular form. The real and imaginary parts of the fundamental at sample point k are calculated by the algorithm using the follows equations:

$$I_{re} = \frac{1}{N} \left[i_{+,k-N} + i_{+,k} + 2 \sum_{\ell=1}^{N-1} i_{+,k-N+\ell} \cos \frac{(2\pi\ell)}{N} \right]$$

$$I_{im} = \frac{1}{N} \left[-2 \sum_{\ell=1}^{N-1} i_{+,k-N+\ell} \sin \frac{(2\pi\ell)}{N} \right]$$
(5.56)

5.5.1 <u>Determination of pps current direction</u>

Of the real and imaginary parts of the fundamental component, only the imaginary part is used for the determination of the pps current direction. The value of the imaginary part is compared with zero to determine the direction of the pps current. If the value of the imaginary part is greater than zero, the pps current flow is consid-

ered to be in one direction; whereas if the value is less than zero, the direction is considered to be opposite. In other words, a positive value of the imaginary part represents one direction; whereas a negative value represents the opposite as described in section 4.2.2 of chapter 4. The important point here is that the imaginary part will always have some magnitude (either positive or negative according to the chosen reference direction and the actual current direction) as long as the system's power factor is other than unity, which is usually the case under both normal operating and fault conditions. So the directions of currents at positions 1, 2, 3 and 4 are determined from the signs (i.e. positive or negative) of the imaginary parts at the corresponding positions.

5.6 Fault detection and location logic

The signs of the imaginary parts at the selected positions, which indicate the current directions at the corresponding positions, are then passed to the final part of the simulation, which is called Fault Detection and Location Logic (FDLL). As explained in chapter 4, there is a unique combination of directions of currents at four selected positions for each condition viz. normal operation with power import and power export, fault at bus 1, the generator circuit and so on. The possible combination of these directions are shown in the Table (5.1). By identifying the combination of these current directions, the FDLL provides the decision on whether a fault has occurred and where it has occurred. Faults at bus 2 and bus 3 of the simulated system under consideration will be referred to as faults

Table-5.1 : Combination of current directions describing the system condition.

	Magnitude of imaginary component of pps current , I_{im} , at positions				20 00 00
case	1	2	3	4	System condition
1	. I _{im} <0	0 <i<sub>im<1.4</i<sub>	I _{im} <0	I _{im} <0	No fault (power exported)
2	I _{im} <0	. O <i<sub>im<1.4</i<sub>	I _{im} >0	. I _{im} >0	No fault (power imported)
3	I _{im} <0	0 <i<sub>im<1.4</i<sub>	I _{im} =0	I _{im} =0	No fault (load & generation are equal)
4	. I _{im} <0	. I _{im} <0	I _{im} >0	. I _{im} >0	. fault at bus l
5	I _{im} =0	. I _{im} <0	. I _{im} >0	I _{im} >0	fault at bus l (generator not connected)
6	I _{im} <0	. I _{im} <0	I _{im} <0	I _{im} >0	. fault at link
7	I _{im} <o< td=""><td>. I_{im}<0</td><td>. I_{im}<0</td><td>. I_{im}<0</td><td>fault at utility</td></o<>	. I _{im} <0	. I _{im} <0	. I _{im} <0	fault at utility
8	I _{im} >0	I _{im} <0	. I _{im} >0	I _{im} >0	fault at generator circuit
9	I _{im} <0 .	I _{im} >1.4	. I _{im} >0	I _{im} >0	fault at motor circuit
10	I _{im} =0	I _{im} >.75	I _{im} >0	I _{im} >0	fault at motor circuit (gen. not connected)

Note: The conditions presented in this table for the determination of system conditions are based on the assumption that the system operates under lagging power factor.

at the link and the utility, respectively, hereafter. There might be a situation, immediately after a fault inception in particular, when the combination of current directions would be different from those shown in the Table (5.1). This situation might last for a very short period of time (1 to 5 samples i.e. 1.66 to 8.33 msec) or for a longer period depending on the type and location of the fault. How the FDLL behaves under these situations will be discussed in the next chapter.

Having received the decision from the FDLL, the algorithm will go back to repeat the process for the next sample. The detailed flow diagram is shown in Fig. 5.9.

5.7 <u>Identification of type of fault</u>

As stated in section 4.3 of chapter 4, after detecting a fault and locating its position on the system, the type of fault can also be determined from off-line analysis of the postfault phase currents. The determination of status of each phase current and zero sequence current is the key feature of this analysis. These status are evaluated through the following steps. Firstly, the magnitude of the maximum current, I_{max} , amongst the three phase currents I_a , I_b and I_c is evaluated. Then, if the ratio of the magnitude of each phase current to I_{max} is greater than a preselected constant, C_1 , the corresponding phase is set to status "1", otherwise it is set to status "0". Similarly, if the ratio of the magnitude of the zero sequence current to I_{max} is greater than another preselected constant.

stant, C_2 , the zero sequence is set to status "1", otherwise it is set to status "0". The way the values of C_1 and C_2 have been selected for this work can best be illustrated by the following example. The phase and zero sequence currents at position 3 for a double line-to-ground (B-C-ground) fault through 0.3α arc resistance at bus 1 of the simulated system, shown in Fig. 5.2, are given below. It is assumed that the system is operating with 20 MVA generation and 30 MVA motor load prior to the fault.

$$I_a = 0.6182122 \ \underline{/106.92}^\circ \quad pu$$
 $I_b = 3.1821817 \ \underline{/-155.41}^\circ \quad pu$
 $I_c = 3.7883149 \ \underline{/49.77}^\circ \quad pu$
 $I_0 = 0.7496724 \ \underline{/106.19}^\circ \quad pu$

From the fault type identification criterion described in chapter 4, the status of phase and zero sequence currents for the example under consideration are known. These are as follows: The status of phase b and c and zero sequence currents are "1" and that of phase a is "0". According to the procedure for the determination of status of phase and zero sequence currents, described earlier, the magnitude of the maximum current, I_{max} , amongst the phases is determined first. In this case

$$I_{max} = 3.7883149$$

Then, the ratio of the magnitude of each phase current to I_{max} is determined as follows

$$I_a/I_{max} = 0.6182122/3.7883149 \approx 0.163$$

 $I_b/I_{max} = 3.1821817/3.7883149 \approx 0.84$
 $I_c/I_{max} = 3.7883149/3.7883149 = 1.0$

Now, a value of \mathbf{C}_1 is to be selected by looking at the above three ratios such that

- i) I_a/I_{max} is less than C_1 , i.e. status of phase a is "0"
- ii) I_b/I_{max} is greater than C_1 , i.e. status of phase b is "1"
- iii) I_c/I_{max} is greater than C_1 , i.e. status of phase c is "1"

It is, therefore, clear that the value of C_1 must be less 0.84 but greater than 0.163. So the value of C_1 can be chosen as 0.83 (for example).

Next, the ratio of the magnitude of zero sequence current to \mathbf{I}_{max} is evaluated as follows

$$I_0/I_{max} = 0.7496724/3.7883149 \approx 0.198$$

Then, a value of C_2 is to be selected such that

 $I_0/I_{\rm max}$ is greater than C_2 , i.e. status of zero seq. is "1" Therefore, the value of C_2 must be less than 0.198 and so it can be selected as 0.19 (for example). The values of C_1 and C_2 thus selected are acceptable only for this example.

However, it has been observed from the results of fault analysis that the constants C_1 and C_2 can vary with the types of faults and prefault conditions. Using the above procedure, the constants C_1 and C_2 have been selected as 0.65 and 0.15 respectively which satisfy the Fault Type Identification Algorithm (FTIA) under all types of faults with different prefault conditions. The flow-chart of FTIA is shown in Fig. 5.10. Having selected these constants, simple condi-

tions, shown in the following Table 5.2, are applied to determine the status of each phase and zero sequence currents.

Table 5.2: Conditions related to the determination of the status of phase and zero sequence currents.

conditions	status		
$\frac{I_a}{I_{max}} > .65$	phase a = 1		
$\frac{I_a}{I_{\text{max}}}$ < .65	phase a = 0		
$\frac{I_b}{I_{max}} > .65$	phase b = 1		
$\frac{I_b}{I_{max}}$ < .65	phase b = 0		
$\frac{I_c}{I_{max}} > .65$	phase c = 1		
$\frac{I_c}{I_{max}}$ < .65	phase c = 0		
$\frac{I_0}{I_{\text{max}}} > .15$	zero seq. = 1		
$\frac{I_0}{I_{\text{max}}} < .15$	zero seq. = 0		

Depending on the location of a fault, the phase currents at a particular monitoring position are used for the determination of the type of fault. For example, if a fault occurs on bus 1, the generator circuit or on the motor circuit, the phase currents of position 3 are used. This choice has been made for the following reasons. Firstly, if, for any reason, the local generation remains disconnected during the fault, phase currents at position 1 are not available. Consequently, the fault type identification becomes impossible using the currents at the above position in this situation. Secondly, it is impossible to identify a ground fault on bus 1 or on the generator circuit by using the currents at position 2 since the ungrounded motor winding causes the zero sequence current to be unavailable at this position for the above fault.

For faults on the high voltage side of the link, the currents at position 4 are used to identify the type of fault, whereas the currents at position 3 are used for faults on the low voltage side. The following simple test can be used to determine whether the fault is on the high or on the low voltage side of the link. If the value of current in the phase carrying the greatest current at position 4 is greater than at least twice that at position 3, the fault is on high voltage side; otherwise it is on the low voltage side. This relationship has been established from the results of fault analysis. However, the FTIA under discussion considers the faults only on the high voltage side of the link.

Since the high voltage winding of the interface transformer is delta connected, the zero sequence current is not available at position 3

or 4 for faults on the utility side. Thus, the types of faults, ground faults in particular, on the utility side cannot be identified.

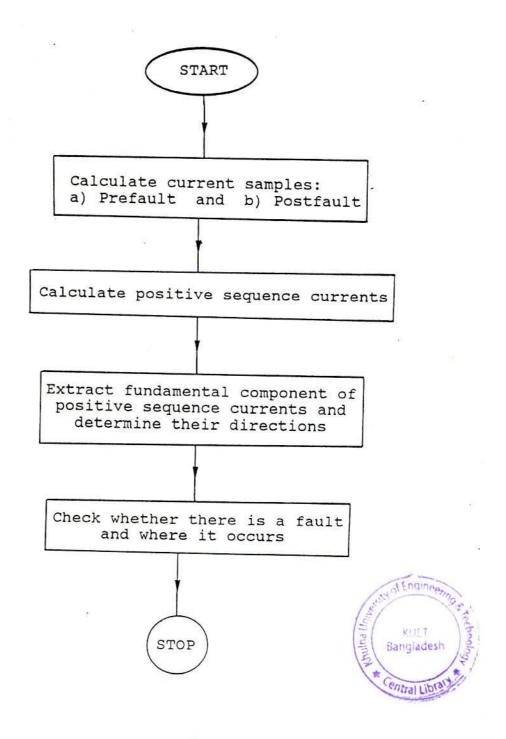


Figure 5.1: Flow-chart showing the main parts of the digital simulation used to test the proposed technique.

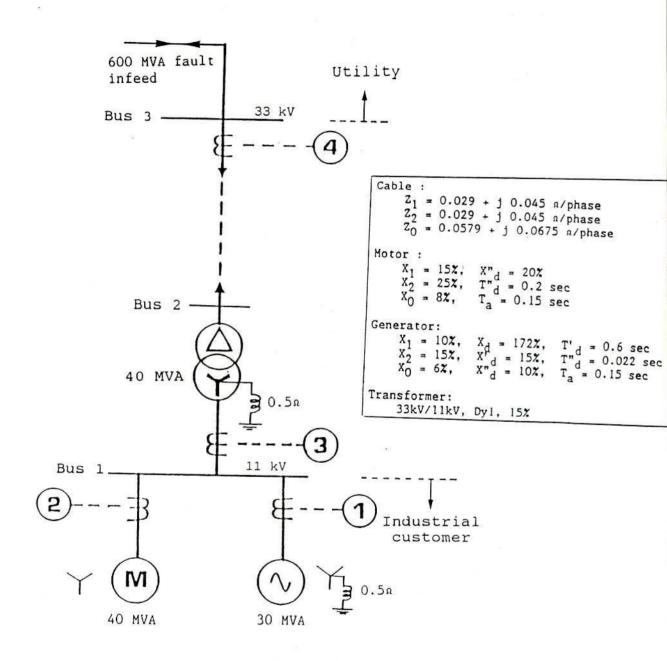
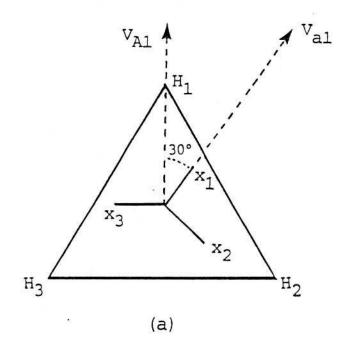


Figure 5.2: The simulated utility interconnected industrial cogeneration system.



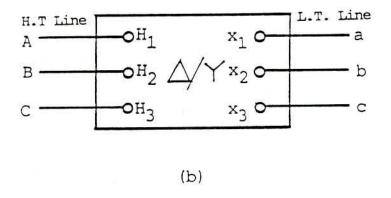
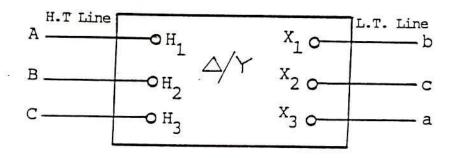
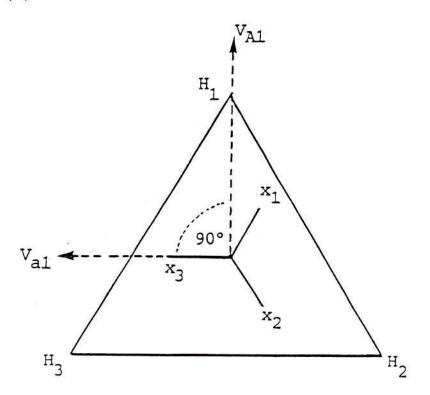


Figure 5.3: a) Positive sequence voltage vector diagram of a Dyl connected transformer.
b) Phase to terminal connections of the

transformer.



(a)



(b)

Figure 5.4: a) Phase to terminal connections of a Dyl connected transformer.

b) Positive sequence voltage vector diagram for connection configuration of (a).

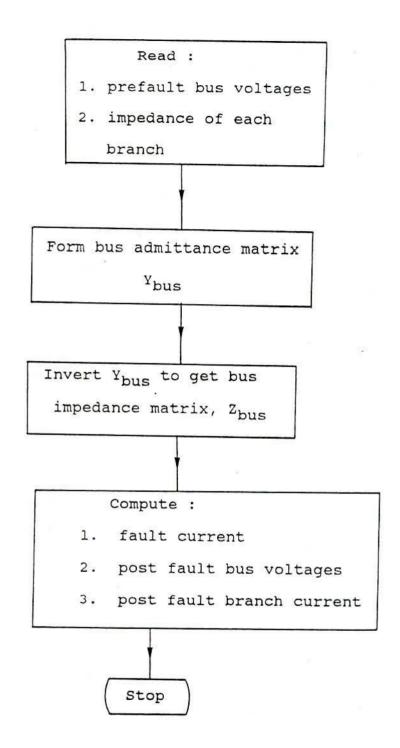


Figure 5.5: Computational flow diagram for fault analysis of bus impedance matrix method.

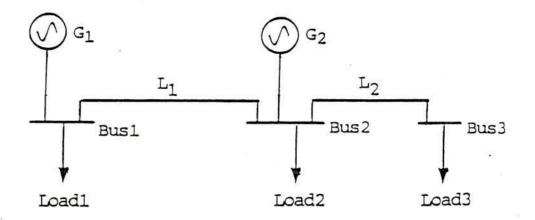


Figure 5.6: Three bus system.

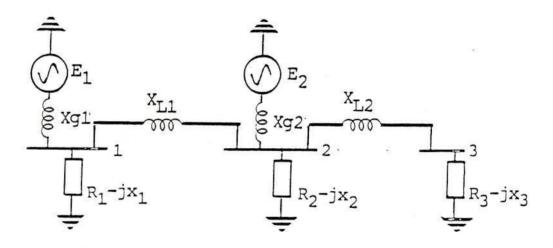


Figure 5.7: Per phase representation of Fig. 5.6.

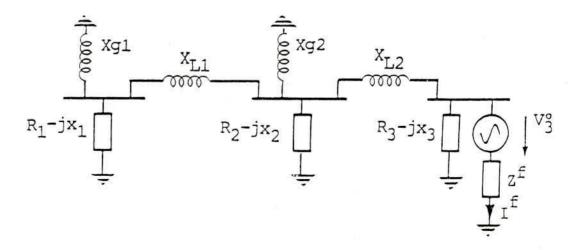
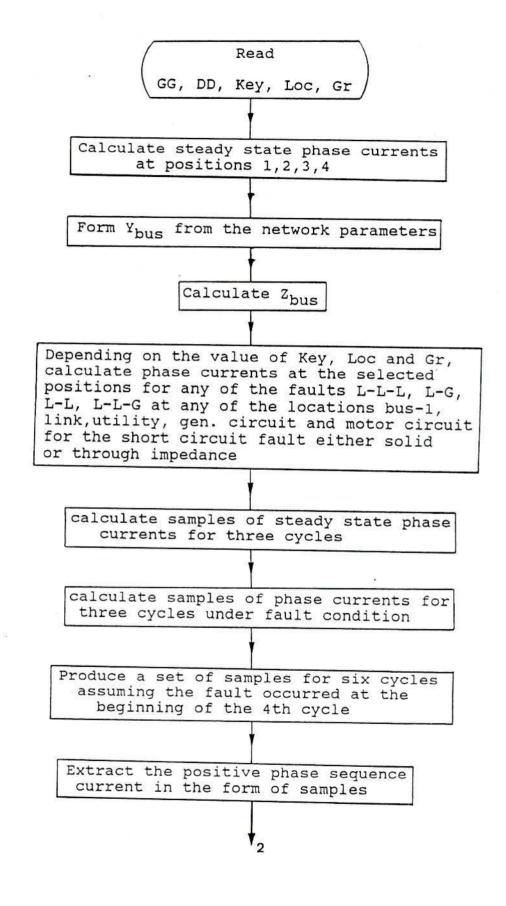


Figure 5.8: Thevenin equivalent circuit of Fig. 5.7.



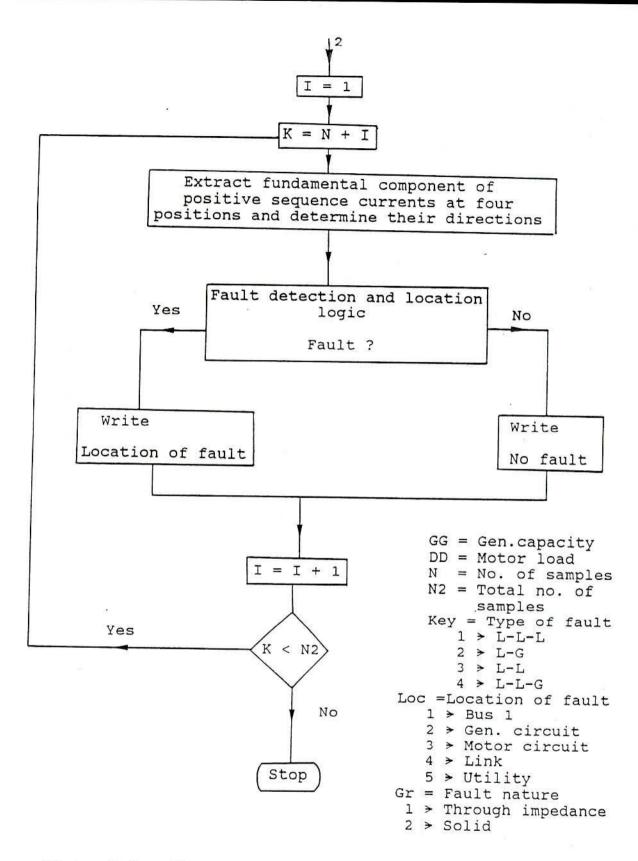


Figure 5.9: Flow-chart of the fault detection and location algorithm.

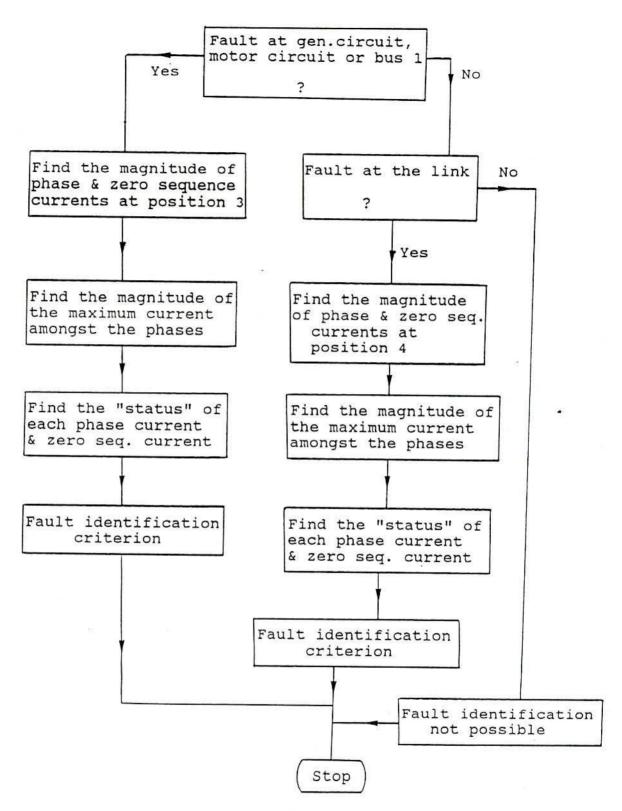


Figure 5.10 : Flow-chart of the fault type identification algorithm.

CHAPTER SIX

RESULTS AND DISCUSSION

6.1 <u>Introduction</u>

In order to detect and locate short circuit faults on a utility interconnected industrial cogeneration system, a new technique has been developed which has the potential for implementation as a microprocessor based protection scheme. In addition, an algorithm, which could easily be incorporated in the protection scheme, has been developed to identify the type of fault by analysing the post fault phase currents. As described in chapter 5, both the interconnected industrial system and the protection scheme have been simulated on a mainframe computer in order to test the validity of the new technique. All types of short circuit faults have been taken into account in the simulation. These include three phase symmetrical, single line-to-ground, line-to-line and double line-to-ground faults. In each case, short circuits, both solid and having arc resistance (or fault path resistance), have been considered. A wide range of prefault operating conditions, including power import and export, has also been considered. The simulated protection scheme has been tested for detection, location and type identification of each type of short circuit fault at different locations on the simulated system, shown in Fig 5.2 of chapter 5. The fault locations include bus 1, the generator circuit, the motor circuit, the link and the utility side.

As explained in chapter 4, the signs of imaginary components (IC) of fundamental pps currents at positions 1, 2, 3 and 4 are used as a means to detect the directions of pps currents at these positions. Having detected these directions, the Fault Detection and Location Logic (FDLL) is used to decide whether a fault has occurred and where it has occurred. The pps current will be referred to as current hereafter. Specimen of test results obtained from the study are presented and discussed in this chapter. For each test, the result includes the behaviour of the IC of currents at four selected positions before and after the fault inception, the outputs of the FDLL and the Fault Type Identification Algorithm (FTIA). In this context, the behaviour of an IC means the variation of its rms value with time. The rms value of IC of each current sample, obtained from the Fourier filtering algorithm, is represented by a point corresponding to the sampling instant. These points, obtained from current samples before and after a fault inception, are joined to get a time varying smooth curve. This will be used to represent the behaviour of an IC. The rms values of IC of currents at positions 1, 2, 3 and 4 will be referred to I_{im1} , I_{im2} , I_{im3} and I_{im4} respectively in rest of this chapter.

6.2 Three phase symmetrical short circuit

Although a wide range of prefault conditions have been considered during the tests of the proposed protection scheme, a sample prefault condition with 30 MVA local generation and 40 MVA motor load is considered here prior to the application of three phase symmetri-

cal faults at different locations. The behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} , and the outputs of FDLL and FTIA for fault with and without arc resistance are presented in the following subsections.

6.2.1 Solid short circuit

Fault at bus 1

Fig. 6.1(a) depicts the behaviours of \mathbf{I}_{im1} , \mathbf{I}_{im2} , \mathbf{I}_{im3} and \mathbf{I}_{im4} before and after the application of a three-phase solid short circuit at bus 1. It is seen that this fault causes the sign of $I_{\text{im}2}$ to change from positive to negative within about a quarter of a cycle from the fault inception. On the other hand, I_{im1} , I_{im3} and I_{im4} increase without changing their signs. This means that the fault causes the current to reverse its direction only at position 2, as expected according to the illustration of currents directions under this condition shown in Fig. 4.1(c) of chapter 4. It is also seen from the figure that after fault inception, the rms values of IC at all positions become much greater than their corresponding values under normal operating conditions. This is again expected because of the fact that the fault currents at those positions become much higher than their prefault values and the system power factor becomes very low during the fault. Consequently, the magnitudes of IC of postfault currents become far more prominent than their real components. Since per unit values of currents at positions 3 and 4 are equal during prefault and postfault (except for fault at the link) conditions, I_{im3} is coincident with I_{im4} , as seen in Fig.

6.1(a). Although the postfault current attains its maximum value in half a cycle following the fault inception in real life, it is seen from Fig. 6.1(a) and indeed following all other cases that the rms values of IC at the selected positions take about one and two third cycles to attain the stable maximum value. The possible reason could be as follows : Although the full cycle Fourier filtering algorithm responds accurately and slowly as samples of highly distorted waveform enter gradually into the data window, its response is not stabilized until its window is completely filled with postfault data. In this study, the positive phase sequence current extraction routine requires a window length of two third of a cycle and the filtering algorithm needs a one cycle window. This means that the filtering algorithm continues to receive mixed samples (i.e. prefault and postfault) into its window upto one and two third cycles after the fault inception. Therefore, after this period the response of the filter becomes stable.

Fig. 6.1(b) shows the computer output of the FDLL. As stated in chapter 5, the sampling frequency is 600 Hz (i.e. 12 samples per cycle of 50 Hz frequency). The fault is applied just after the 12th sample of the current data under consideration. It is seen that the FDLL can not recognise the fault for the next consecutive three samples (i.e. 13, 14 and 15th) after fault inception. However, this figure shows that the fault is detected and located at the 16th sample. Fig. 6.1(c) shows the output of the FTIA which gives the type of the fault. In this case, it has indicated that the fault is a "three phase fault", as expected.

Fault at the generator circuit

Fig. 6.2(a) depicts the behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a three phase solid fault at the generator circuit. Due to the fault, the sign of I_{iml} has been changed from negative to positive, and that of I_{im2} from positive to negative. I_{im3} and I_{im4} , however, have been increased without changing their signs, as expected. It is also evident that \mathbf{I}_{iml} crosses the zero reference line earlier than \mathbf{I}_{im2} . In this situation \mathbf{I}_{im1} becomes positive after crossing the reference line whilst I_{im2} still positive. Under this situation, the combination of signs of $I_{\mbox{iml}}$, $I_{im2},\ I_{im3}$ and I_{im4} (i.e. the combination of current directions) does not resemble any of the combinations shown in Table (5.1) of chapter 5 to describe the system condition. Thus this situation represents neither normal operating nor fault condition. The FDLL has, therefore, been programmed in such a way that it recognises this situation as a non-defined condition and produces a "not defined" in its output. The FDLL will continue to produce this indication until ${ t I}_{ t im2}$ crosses the reference line and becomes negative.

Fig. 6.2(b) shows the output of the FDLL. The fault is applied just after the 12th sample. It is seen that the FDLL gives "no fault" indication for two samples (i.e. 13 and 14th) after the fault inception. On the 15th sample, however, the FDLL recognises the above mentioned non-defined situation and produces "not defined" in its output, as shown in Fig. 6.2(b). In this case, the FDLL takes a quarter of a cycle to detect and locate the fault. Fig. 6.2(c) shows

the output of the FTIA.

Fault at the motor circuit

Fig. 6.3(a) presents the behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a three phase solid fault at the motor circuit. It is seen that due to this fault, all the rms values of IC at the selected four positions have been increased without changing their signs. This indicates that the fault causes the currents at four selected positions to increase in magnitude without changing their directions, which is expected for the prefault condition under consideration. This situation has been explained in chapter 4. Since there are no changes in the directions of currents at any of the positions, even after the fault, the FDLL is supposed to consider this situation as a "no fault" condition. However, as explained in chapter 4, the FDLL recognises this situation as a fault on the motor circuit by comparing the magnitude of $\mathbf{I}_{\text{im}2}$ with a preset threshold. The threshold value is chosen on the basis of the expected maximum current to be drawn by the motor under normal operating conditions.

Fig. 6.3(b) shows the output of the FDLL. It is evident that the fault, applied just after the 12th sample, is detected and located on the 17th sample, i.e. in less than half a cycle. In practical applications, however, the protection scheme must ignore the operation of the relevant circuit breaker during motor starting, when the current drawn by the motor will certainly exceed the preset thresh-

old. This can easily be achieved by introducing a time delay in the trip signal initiated by the FDLL. Fig. 6.3(c) shows the output of the FTIA indicating a "three phase fault" as expected.

Fault at the link

Fig. 6.4(a) shows the behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a three phase solid fault at the link. The fault causes the signs of I_{im2} and I_{im3} to change from positive to negative, whereas I_{im1} and I_{im4} are increased without changing their signs. The I_{im2} takes about half a cycle to cross the zero reference line after the fault inception. It is also noticed that when the I_{im3} crosses the reference line and becomes negative, the magnitude of I_{im2} still remains positive. This situation again represents, as explained earlier, a non-defined condition. The FDLL correctly recognises this situation and produces "not defined" in its output. The FDLL continues to produce this message until $I_{\mbox{im}2}$ crosses the reference line and becomes negative. This is shown in Fig. 6.4(b). There are two noticeable points in Fig. 6.4(a). Firstly, although I_{im3} and I_{im4} are coincident during prefault condition, they are increased with opposite signs following the fault inception. This is expected because current flow at positions 3 and 4 become opposite in direction after this fault. Secondly, the magnitude of $I_{ exttt{im4}}$ is much higher than that of $I_{ exttt{im3}}$. This is because of the fact that the fault current contribution by the utility (measured at position 4) is much higher than that by the industrial plant, i.e. generator and motor, (measured at position 3) for this

fault, which is assumed to be at the high voltage terminals of the interface transformer. Fig. 6.4(c) shows the output of the FTIA.

Fault at the utility

The performance of the protection scheme for a three phase solid short circuit at the utility is presented here. It is seen from Fig. 6.5(a) that I_{im3} and I_{im4} , both of which have equal pu value and thus coincident under prefault and postfault conditions, have crossed the reference line from positive side to negative in less than a quarter of a cycle after the fault inception; whereas $I_{\text{im}2}$ takes a little more than half a cycle to do so. However, changes of signs of I_{im3} and I_{im4} (i.e. changes of current directions at positions 3 and 4) alone does not indicate any fault in the system. The situation during the period, when I_{im3} and I_{im4} have changed from positive to negative but I_{im2} remains positive, represents a normal operating condition with power being exported to the utility. The FDLL correctly recognises the situation as a no fault condition and produces "no fault" message in its output during this period. When $I_{\mbox{im2}}$ crosses the reference line and becomes negative, the FDLL detects the fault and produces a message indicating its location. This is shown in Fig. 6.5(b). For faults at the utility side it is not possible to identify their types, as explained in chapter 4. Thus the FTIA, in this case, produces a message indicating "identification not possible", as shown in Fig. 6.5(c).

6.2.2 <u>Short circuit fault through resistance</u>

Fault at bus 1

The performance of the protection scheme for a three phase short circuit with a fault arc resistance of 0.15n at bus 1 is presented here. It is seen from Fig. 6.6(a) that I_{im2} takes more than half a cycle to change its sign from positive to negative after the fault inception. However, for a three phase solid short circuit at the same location, I_{im2} takes a quarter of a cycle to reverse, as shown in Fig. 6.1(a). Thus the FDLL takes a longer time to detect and locate a three phase short circuit with arc resistance at bus 1 compared with a solid short circuit at the same location. It is also seen here that the magnitudes of $\mathtt{I}_{\mathsf{im}1}$, $\mathtt{I}_{\mathsf{im}2}$, $\mathtt{I}_{\mathsf{im}3}$ and $\mathtt{I}_{\mathsf{im}4}$ are considerably lower than in the case of solid fault, shown in Fig, 6.1(a). This is an obvious consequence of the presence of arc resistance in the fault path, which reduces the magnitude of fault current at each position. This fault path resistance along with dc offsets, present in the fault current contributions by the generator and the motor, cause \mathbf{I}_{iml} and \mathbf{I}_{im2} , in particular, to fluctuate prominently after half a cycle following the fault inception, as shown in Fig. 6.6(a). However, the output of the Fourier filtering algorithm (i.e. I_{im1} , I_{im2} , etc.) becomes gradually stable as the filter's window is gradually filled with fault current data.

Fig. 6.6(b) shows the response of the FDLL due to this fault, which is assumed to occur just after the 12th sample. The fault is detected and located at the 21st sample. The FDLL continues to produce a

"no fault" message during the period from 13th sample to 20th sample. However, the FDLL can detect and locate a three phase solid fault at the same location on the 16th sample, as shown in Fig. 6.1(b). The FTIA correctly produces a message indicating "three phase fault" as shown in Fig. 6.6(c).

Fault at the generator circuit

The performance of the protection scheme has been tested with the application of a three phase short circuit with a fault path resistance of 0.15 n at the generator circuit. The test results are presented here. It is seen from Fig. 6.7(a) that this fault causes the signs of IC at the selected positions to vary in the same way as for the case of a solid fault, shown in Fig. 6.2(a). However, I_{iml} and I_{im2} take longer time to cross the zero reference line after the fault inception compared with the case of a solid fault. This again indicates that the scheme becomes slower in detecting and locating a fault with arc resistance.

Fig. 6.7(b) shows the response of the FDLL before and after the application of the fault. It is seen that after the fault inception, the FDLL produces "no fault" message as long as $I_{\rm iml}$ does not cross the reference line from negative side to positive, i.e. its sign remains negative. When the sign of $I_{\rm iml}$ becomes positive, at the 16th sample, the FDLL starts to indicate a "not defined" condition and continues to do so as long as the sign of $I_{\rm im2}$ remains positive. When $I_{\rm im2}$ crosses the reference line and becomes negative, i.e. at the 21st sample, the FDLL recognises the fault and its location.

Fig. 6.7(c) shows the output of the FTIA.

Fault at the motor circuit

Fig. 6.8(a) depicts the behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a three phase short circuit having a fault path resistance of 0.15α at the motor circuit. As a result of this fault, the magnitudes of IC at all selected positions have been increased without changing their signs, as also happened in the case of a solid fault, as discussed earlier. However, Fig. 6.8(b) shows that the fault, occurring just after the 12th sample, has been detected and located at the 21st sample; whereas the solid fault has been detected at the 17th sample, as shown in Fig. 6.3(b). The output of the FTIA is shown in Fig. 6.8(c).

Fault at the link

The behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} due to the application of a three phase short circuit through 1.0α fault resistance at the link are shown in Fig. 6.9(a). The magnitudes of I_{im1} and I_{im4} have been increased without changing their signs after the fault inception. I_{im3} crosses the reference line and becomes negative for a very short period of time. The FDLL recognises this period (samples 16 and 17, shown in Fig. 6.9(b)) as a non-defined condition. I_{im3} then reverts to positive magnitude and remains there for another period of time, indicating a "no fault" condition (sample 18 and 19). I_{im3} again crosses the reference line and finally becomes

negative while I_{im2} is still positive. In this situation, the combination of signs of IC at the selected positions again represents a non-defined condition. So, the FDLL continues to produce a "not defined" message until I_{im2} crosses the reference line and becomes negative. These situations are shown in Fig. 6.9(b). It is seen that the FDLL detects the fault and locate its position at the 22nd sample. As explained earlier, the fault path resistance and do offsets present in the generator and motor fault currents are the cause of the fluctuation of I_{im3} after half a cycle following the fault inception, as shown in Fig. 6.9(a). It has also been observed during the tests that this fluctuation becomes more prominent with the increase in fault path resistance. However, I_{im3} becomes stable in less than one cycle even with increased fault path resistance enabling the FDLL to detect and locate the fault in less than one cycle. The output of FTIA is shown in Fig. 6.9(c).

Fault at the utility

The performance of the proposed scheme for a three phase short circuit through 1.0a fault resistance at the utility side is presented in Fig. 6.10. It is seen from Fig. 6.10(a) that this fault causes the magnitudes of IC at all the selected positions to change in the same way as occurred in the case of solid fault, shown in Fig. 6.5(a). However, it is evident from Fig. 6.10(b) that the FDLL takes longer time to detect and locate this fault than for a solid fault. The output of FTIA is shown in Fig. 6.10(c).

6.3 <u>Unsymmetrical faults</u>

The performance of the algorithms for the proposed protection scheme has been found satisfactory for all kinds of unsymmetrical faults at different locations with different prefault operating conditions, including power import and export. However, in order to avoid repetition, samples of test results of unsymmetrical faults only at the link have been presented in this section.

6.3.1 Single line-to-ground fault

6.3.1.1 Solid fault

The variations of I_{im1} , I_{im2} , I_{im3} and I_{im4} are shown Fig. 6.11(a) before and after the application of a single line-to-solid ground fault at the link. The system, prior to the application of the fault, is assumed to operate with 30 MVA of generation and 20 MVA of motor load, i.e. power being exported by the industrial customer. The fault causes I_{im2} and I_{im4} to reverse their signs, as expected. It is also seen from Fig. 6.11(a) that while I_{im4} requires less than a quarter of a cycle to cross the reference line, I_{im2} takes about a cycle to do so. The FDLL starts to indicate a non-defined condition when I_{im4} crosses the reference line and continues to do so until I_{im2} crosses the reference line. The FDLL takes about a cycle to detect and locate the fault, as shown in Fig. 6.11(b). The FTIA produces a message indicating the type of the fault, as shown in Fig. 6.11(c).

Fig. 6.12 shows the performance of the scheme for the same type of fault at the same location but with 30 MVA of generation and 40 MVA of motor load (i.e. power being imported) prior to the fault. It is seen from Fig. 6.12(a) that the signs of I_{im2} and I_{im3} , instead of I_{im2} and I_{im4} as happened in the previous case, have been reversed due to this fault. This is again expected as explained in chapter 4. I_{im3} takes less than half a cycle to cross the reference line; whereas I_{im2} requires more than a cycle. Fig. 6.12(b) shows that the FDLL takes more than a cycle to detect and locate the fault. The output of FTIA is given in Fig. 6.12(c).

6.3.1.2 <u>Fault through resistance</u>

Fig. 6.13(a) depicts the behaviours of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a single line-to-ground fault through 1.0a fault resistance at the link. Prior to the fault, the system is assumed to operate with 30 MVA generation and 20 MVA motor load. It is evident that I_{im4} crosses the reference line almost immediately after the fault, whereas I_{im2} takes about one and a quarter cycles. Comparing this case with that of the solid fault under the same prefault condition, shown in Fig. 6.11(a), it is apparent that a longer time is required to detect and locate a single line to ground fault through resistance than for a solid fault. Fig. 6.13(b) shows that the fault, applied after the 12th sample, has been detected and located by the FDLL at the 28th sample. The FTIA correctly recognises the type of the fault and produces a message, as shown in Fig. 6.13(c).

Fig. 6.14 shows the performance of the scheme for a single line- toground fault having 0.5 n of fault path resistance at the same location but with 30 MVA generation and 40 MVA motor load prior to the fault. Comparing this with the performance of the solid fault under the same prefault condition, shown in Fig. 6.12, it can be again concluded that the FDLL requires more time to detect and locate a fault through resistance than a solid fault.

6.3.2 <u>Line-to-line fault</u>

6.3.2.1 Solid fault

The variations of I_{im1} , I_{im2} , I_{im3} and I_{im4} before and after the application of a line-to-line solid short circuit at the link are shown in Fig. 6.15(a). The system is assumed to operate with 20 MVA generation and 10 MVA motor load prior to the fault. After the fault inception, I_{im2} crosses the reference line in about half a cycle, whereas I_{im4} does so in less than half a cycle. Fig. 6.15(b) shows that the fault is applied just after the 12th sample and detected and located at the 20th sample. The output of the FTIA is shown in Fig. 6.15(c).

Fig. 6.16 illustrates the performance of the scheme for the same type of fault at the same location but with 20 MVA generation and 30 MVA motor load prior to the fault. In this case, the fault causes I_{im2} and I_{im3} , instead of I_{im2} and I_{im4} as for the previous case, to reverse their signs as shown in Fig. 6.16(a). It is evident from

Fig. 6.16(b) that the fault is detected and located at the 21st sample. The output of FTIA is shown in Fig. 6.16(c).

Comparing the above two cases, presented in Figs. 6.15 and 6.16, it is apparent that the fault detection and location time also varies slightly with the variation of prefault conditions (i.e. variation of generation and motor load).

6.3.2.2 <u>Fault through resistance</u>

Fig. 6.17 presents the performance of the protection scheme algorithms for a line-to-line short circuit through 2.0s fault resistance at the link with 20 MVA generation and 10 MVA motor load in the system prior to the fault. It is evident from Fig. 6.17(a) that due to the fault the sign of $I_{\rm im4}$ is changed from negative to positive in less than half a cycle; whereas that of $I_{\rm im2}$ goes from positive to negative in about three quarters of a cycle. Fig. 6.17(b) shows that the fault, applied just after the 12th sample, is detected and located at the 22nd sample. This means that the algorithm takes about three quarters of a cycle to detect the fault after its inception. In the case of a solid line-to-line fault under the above prefault condition, shown in Fig. 6.15, the algorithm, however, takes about half a cycle to do so. Therefore, it can again be concluded that solid faults are detected and located faster than faults through resistance.

If the fault path resistance is very high, the algorithm cannot detect the fault. The performance of the scheme under such a high

resistance fault is shown in Fig. 6.18. The behaviours of I_{iml} , I_{im2} , I_{im3} and I_{im4} before and after the application of a line-to-line fault through 6.0a fault resistance at the link are shown in Fig. 6.18(a). Prior to the application of the fault, the system is assumed to operate with 20 MVA generation and 10 MVA motor load. It is evident from Fig. 6.18(a) that the fault causes the sign of I_{im4} to change from negative to positive but gives no change of sign of I_{im2} . It indicates that there is no change in the current direction at position 2. After the application of this sort of high resistance fault, the voltage of bus 1 remains higher than the internal emf of the motor. So the motor does not contribute any current to the fault, rather it continues to consume power from bus 1 as a load, keeping the current direction at position 2 unchanged. Therefore, the FDLL cannot detect the fault, rather it continues to produce a message indicating non-defined condition.

The maximum value of fault path resistance, for which the FDLL is just able to detect and locate different types of faults, will be discussed in section 6.4. The approximate value of possible arc resistance [36,42] for the voltage level under discussion has been found to be less than the above maximum value of the fault path resistance. Hence, it is expected that the proposed protection scheme will work satisfactorily under all possible arcing fault conditions.

6.3.3 <u>Double line-to-ground fault</u>

6.3.3.1 Solid fault

Fig. 6.19(a) presents the behaviours of I_{lm1} , I_{lm2} , I_{lm3} and I_{lm4} for a double line-to-solid ground fault at the link while the system is assumed to operate with 20 MVA generation and 30 MVA motor load prior to the fault. It is seen from Fig. 6.19(a) that I_{lm3} crosses the reference line in less than a quarter of a cycle after the fault inception while I_{lm2} and I_{lm4} remain on the positive side, representing a non-defined condition (i.e. 15th sample of Fig. 6.19(b)). However, I_{lm4} just crosses the reference line and becomes negative for a very short period of time while I_{lm2} is still on the positive side. This period indicates a "no fault" condition (i.e. 16th sample). The situation again becomes non-defined when I_{lm4} becomes positive and I_{lm2} remains positive. This situation is continued until I_{lm2} crosses the reference line and becomes negative. These are shown in Fig. 6.19(b). The output of the FTIA is shown in Fig. 6.19(c).

Fig. 6.20 illustrates the performance of the algorithms for the same type of fault at the same location but with 30 MVA generation and 20 MVA motor load in the system prior to the fault. It is evident from Fig. 6.20(a) that the magnitudes of I_{im1} and I_{im3} are increased without changing their signs after the fault inception; whereas I_{im4} crosses the reference line from the negative side to the positive and I_{im2} from positive side to the negative. Fig. 6.20(b) shows that the fault, applied just after the 12th sample, is detected and located at the 20th sample. The output of the FTIA is shown in Fig. 6.20(c).

6.3.3.2 Fault through resistance

Fig. 6.21 presents the performance of the algorithms for a double line-to-ground fault through 3.0 fault resistance at the link. Prior to the application of the fault, the system is assumed to operate with 30 MVA generation and 20 MVA motor load. Comparing the output of FDLL, shown in Fig. 6.21(b) with that shown in Fig. 6.20(b), it is clear that the algorithm can detect and locate double line-to-solid ground faults quicker than faults through resistance.

The algorithm, however, cannot detect a double line-to-ground fault through very high resistance. The performance of the scheme under such a high resistance fault condition is shown in Fig. 6.22. The behaviours of $I_{\rm im1}$, $I_{\rm im2}$, $I_{\rm im3}$ and $I_{\rm im4}$ for a double line-to-ground fault through 7.00 fault resistance at the link are shown in Fig. 6.22(a). The system is assumed to operate with 30 MVA generation and 20 MVA motor load prior to the fault. It is seen that $I_{\rm im4}$ crosses the reference line in little more than half a cycle after the fault inception, but $I_{\rm im2}$ does not cross the reference line at all. This indicates that the motor does not contribute any fault current under this situation, as explained earlier. So, the algorithm continues to indicate this situation as non-defined condition but cannot detect the fault.

Situations have also been found during the tests when the algorithm continues to indicate a "no fault" condition in its output for a very high resistance fault in the system; for example, a double line-to-ground fault through $7.0 \, \text{n}$ fault resistance at the utility

side irrespective of prefault conditions. The performance of the algorithms for the above situation, however, is not shown here.

6.4 <u>Discussion</u>

The proposed algorithms for the protection scheme have been tested with all kinds of short circuit faults, both solid and through resistance, and under different operating conditions, both import and export, prior to the fault. The following observations have been made from the tests. Firstly, the time required by the FDLL to detect and locate a fault depends on many factors, such as type, location and nature (i.e. solid or through resistance) of the fault and the prefault condition (i.e. amount of generation and motor load). Secondly, the FDLL takes longer to detect a resistive fault than a solid one. Thirdly, three phase faults can be detected and located in much less time than that required for single line-to-ground faults in general. Finally, in the case of solid short circuits in particular, the fault detection and location time is a maximum for a single line-to-ground fault and progressively lower for line-to-line, double line-to-ground and three phase faults.

It has also been observed that solid and low resistance faults can confidently be detected and located well within one cycle from the fault inception, particularly three phase, double line-to-ground and line-to-line faults. Single line-to-ground faults, however, require just over a cycle to be detected and located. The FDLL cannot detect a short circuit fault through very high resistance. In the case of high resistance faults on bus 1, the motor circuit and the utility,

the FDLL continues to produce a "no fault" message. However, the FDLL continues to indicate a "not defined" condition after the inception of faults at the generator circuit or the link. Hence, this condition, indicating abnormalities somewhere in the system, could be brought to the operator's notice by activating an alarm signal after receiving consecutive twelve samples, for example, of "not defined" output from the FDLL.

It has been revealed from the tests that the value of fault path resistance, for which the FDLL can detect and locate the fault, depends on the system's prefault condition, the amount of motor load in particular. The higher the motor load in the system prior to the fault, the lower is the maximum fault path resistance for which fault detection is possible. The amount of generation has a negligible effect. The possible reason may be explained as follows: As stated in chapter 5, the reversal of current direction at position 2 (i.e. fault current contribution by the motor) is one of the necessary conditions for a fault to be detected and located by the FDLL. As the load increases, the internal emf of the motor decreases. Under this condition, the motor only contributes fault current to any fault on the system when the postfault bus 1 voltage becomes lower than the internal emf of the motor. This essentially requires a lower fault path resistance. The amount of prefault generation, incidentally, does not have much effect on whether the motor contributes fault current or not under such conditions. For different kinds of faults at different locations under maximum and minimum prefault loading conditions, the maximum value of fault path resistance, for which the FDLL is just able to detect and locate the faults, have been found from the tests and are presented in table 6.1.

Since faults at bus 1, the generator circuit and the motor circuit are electrically very close, it is logical to conclude that the FDLL should detect and locate these faults having the same fault path resistance. However, it is evident from Table 6.1 that the maximum fault path resistance for detection of a fault on the motor circuit is less than those at bus I and on the generator circuit for each type of fault and each prefault loading condition. As a matter of fact, the detection and location of faults on the generator circuit and bus 1 depend on the reversal of current direction at position 2. As stated earlier, this reversal only takes place when the internal emf of the motor is higher than the postfault voltage at the fault points i.e. at bus 1 and the generator circuit which are, indeed, electrically very close. This means that postfault voltages at bus 1 and the generator circuit for faults on these locations can safely be considered as the same. This is, of course, possible only if the fault path resistances for faults on these locations (i.e. bus 1 and the generator circuit) are the same. This has also been found from the tests. On the other hand, detection and location of faults on the motor circuit does not, at all, depends on the reversal of current direction at position 2; rather faults at this location (on the motor circuit) are determined by comparing the magnitude of Iim2 with a preset threshold. Hence, the lower the fault path resistance, the higher is the magnitude of I_{im2} and consequently, the higher could be the threshold value and vice-versa. This means that the

Table 6.1: The maximum fault path resistance for which the FDLL can just detect and locate the fault.

Type of fault	Prefault motor load (in MVA)	Location of fault	Fault path resistance (in ohm)
Single line to ground fault	40	Bus 1 Gen. circuit Motor circuit Link Utility	0.41 0.41 0.31 1.02 1.0
	10	Bus 1 Gen. circuit Motor circuit Link Utility	0.55 0.55 0.316 1.60 1.55
Line to line fault	40	Bus 1 Gen. circuit Motor circuit Link Utility	0.89 0.89 0.79 3.20 3.10
	10	Bus 1 Gen. circuit Motor circuit Link Utility	1.20 1.20 0.87 4.60 4.50
Double line to ground fault	40	Bus 1 Gen. circuit Motor circuit Link Utility	1.13 1.13 0.98 4.00 3.91
	10	Bus 1 Gen. circuit Motor circuit Link Utility	1.53 1.53 1.10 5.72 5.55
Three phase Eault	40	Bus 1 Gen. circuit Motor circuit Link Utility	0.60 0.60 0.49 2.53 2.46
	10	Bus 1 Gen. circuit Motor circuit Link Utility	0.82 0.82 0.56 3.70 3.60

maximum fault path resistance, shown in Table 6.1, for detection of a fault on the motor circuit could be increased by lowering the threshold value. This has, also, been confirmed by the results of the test. The Table 5.1 of chapter 5 shows that the threshold value has been chosen as 1.4 pu when the local generator is connected to the industrial system, and as 0.75 pu when the generator is not connected. For a fault on the motor circuit, the contribution of the local generator causes a considerable increase in the total fault current at position 2 and thus in the magnitude of I_{im2} . This is the reason why the threshold is set at much higher value in the case when local generator remains connected to the industrial system than for the case when the generator is not connected. It has been observed from the study that the magnitude of $I_{\mbox{im}2}$ is much higher in the case of a three phase fault on the motor circuit than those for unsymmetrical faults on the same location. This essentially means that the threshold could be set at different values depending on the types of fault. However, for this study, two threshold values, as discussed earlier and shown in Table 5.1 of chapter 5, have been chosen such that the FDLL can detect and locate all types of faults with the amount of fault path resistance as shown in Table 6.1. A high threshold value causes delay in the fault detection and increases the possibility of undetection of high resistance faults, in particular; but decreases the risk of detecting the motor starting as a fault on the motor circuit. On the other hand, a low threshold value results in faster fault detection but increases the possibility of detecting the motor starting as a fault on the motor circuit. So, in a practical application, a compromise must be reached to meet

the requirements.

Under balanced condition (normal operating or three phase fault), knowledge of current or voltage in one phase implies knowledge of the corresponding variables on the other two phases because of their complete three phase symmetry. This means that if, for example, the direction of phase "a" current (with respect to phase "a" voltage) at any point on a network is determined, the direction of the variable on the other two phases (with respect to the corresponding phase voltage) can easily be ascertained. However, this is not possible in the case of unsymmetrical faults or unbalanced loading conditions. It is necessary to examine the different phases individually. The complexity and computational time involved in using the phase currents as the parameters of the protection function under consideration gave rise to the idea of using pps current instead. The pps currents in all three phases have a complete symmetry. Thus it is possible to limit the analysis (determination of pps current direction in this study) to one phase only. Since pps volt-amperes always flow to a fault [95], a pps current also flows to a fault either balanced or unbalanced. Determination of direction of pps current is one of the key features of this study. By comparing the phase angle of a pps current at any point on a network with that of pps voltage at the corresponding point, the direction of the pps current could be evaluated. This method, of course, would require the calculation of phase angles of the variables, and thus would require more processing time. The proposed technique, however, does not require to calculate the phase angle; rather it uses only the imaginary part (more precisely the sign of the imaginary part) of the fundamental

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component of pps current for the determination of the pps current direction. The fundamental component of the pps current is extracted in rectangular form, having a real and an imaginary parts, by the digital filter. The sign of the imaginary part is used directly to determine the direction. Thus it saves a considerable amount of processing time.

As stated in chapter 5, the proposed scheme has the ability to use the pps voltage of the industrial busbar (at the low voltage side of the interfacing transformer) to derive the required polarising reference for the determination of pps current direction at position 4 (at the high voltage side of the interface). This saves the cost of a potential transformer at position 4. In addition, the proposed scheme provides differential protection of both the interface link and the industrial busbar, reverse power protection of the local generator and overcurrent protection of the motor feeder. The scheme is, therefore, expected to be cheaper than its conventional counterpart.

For this study, although 12 samples per cycle has been used as the sampling rate, it could be increased to 16 samples per cycle or even more. In fact, the higher the sampling rate, the better is the filtering performance. However, in a real time application, the sampling rate is limited by the number of input signals and the processing time required by the microprocessor. It is expected that the chosen sampling interval (1.666 msec) could be adequate for the processing time with the number of inputs involved in this study.

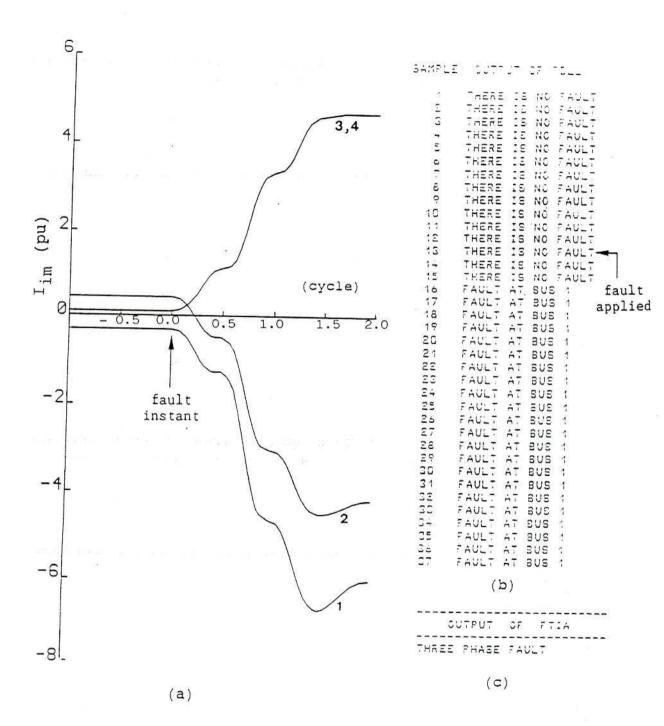


Figure 6.1: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a solid three phase fault at bus 1 with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

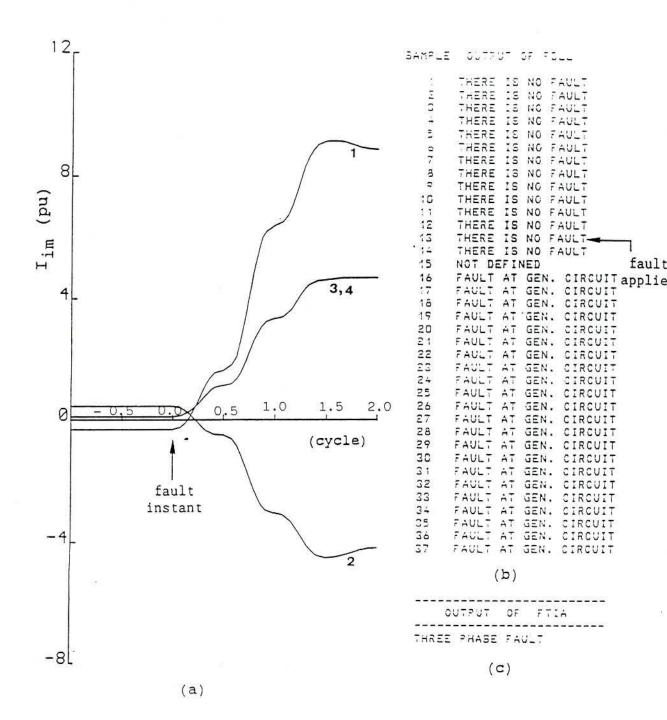


Figure 6.2: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a solid three phase fault at the generator circuit with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

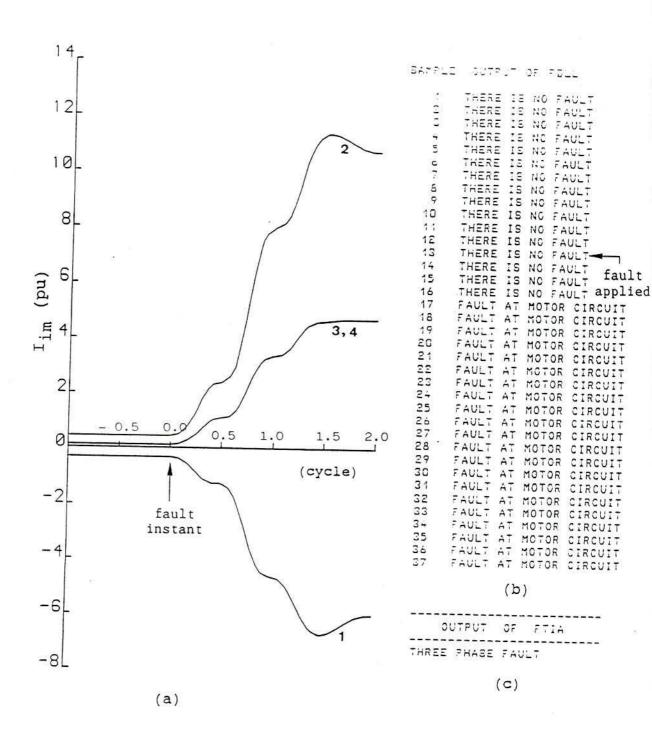


Figure 6.3: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a solid three phase fault on the motor circuit with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

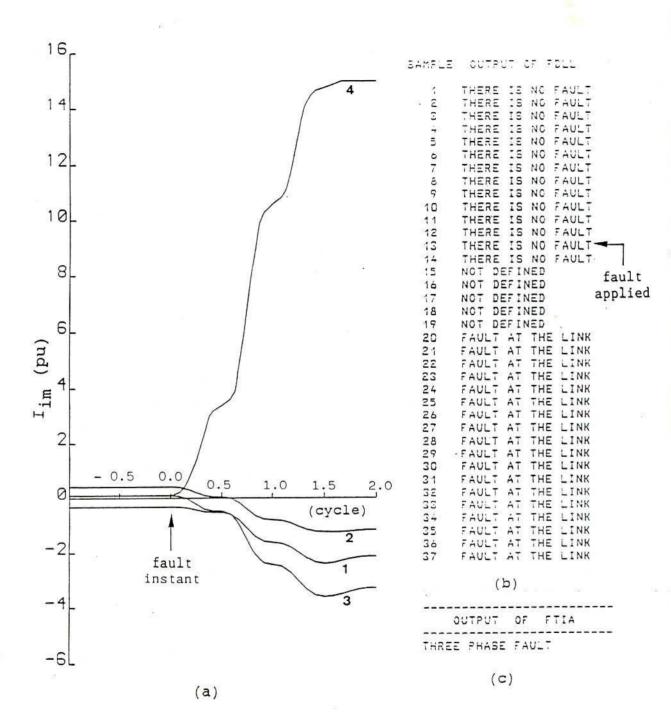
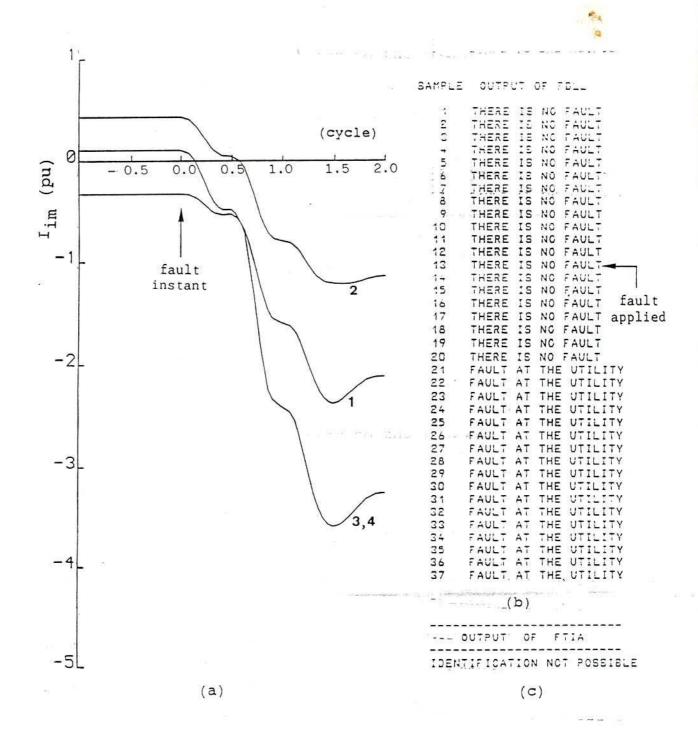


Figure 6.4: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a solid three phase fault at the link with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.



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Figure 6.5: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a solid three phase fault at the utility side with power being imported prior to the fault.

b) Output of FDLL.
c) Output of FTIA.

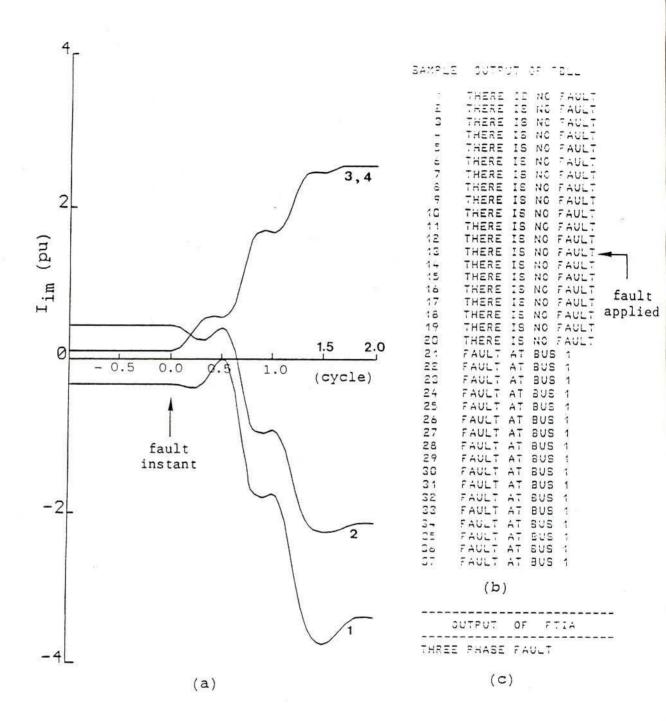


Figure 6.6: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a three phase fault through 0.15% arc resistance at bus 1 with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

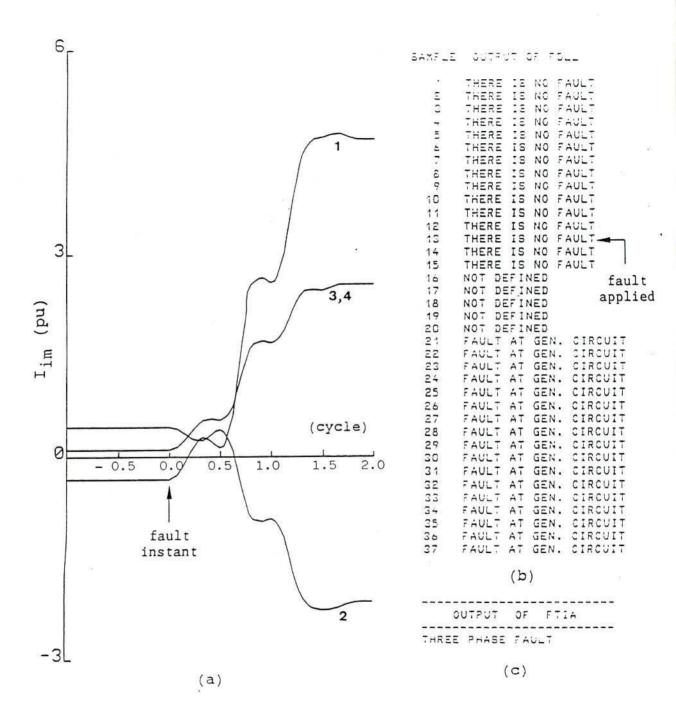


Figure 6.7: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a three phase fault through 0.150 arc resistance at the generator circuit with power being imported prior to the fault.

-b) Output of FDLL.

c) Output of FTIA.

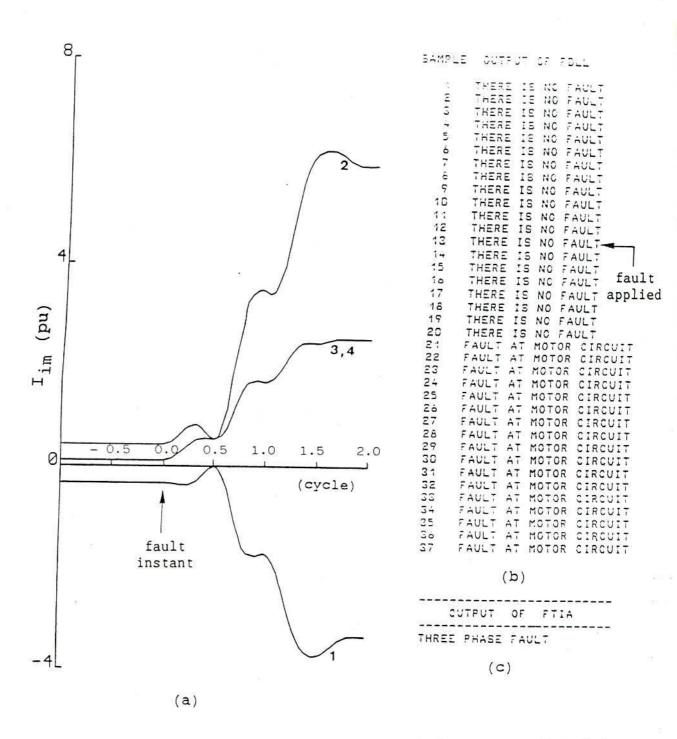


Figure 6.8: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a three phase fault through 0.15 α arc resistance at the motor circuit with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

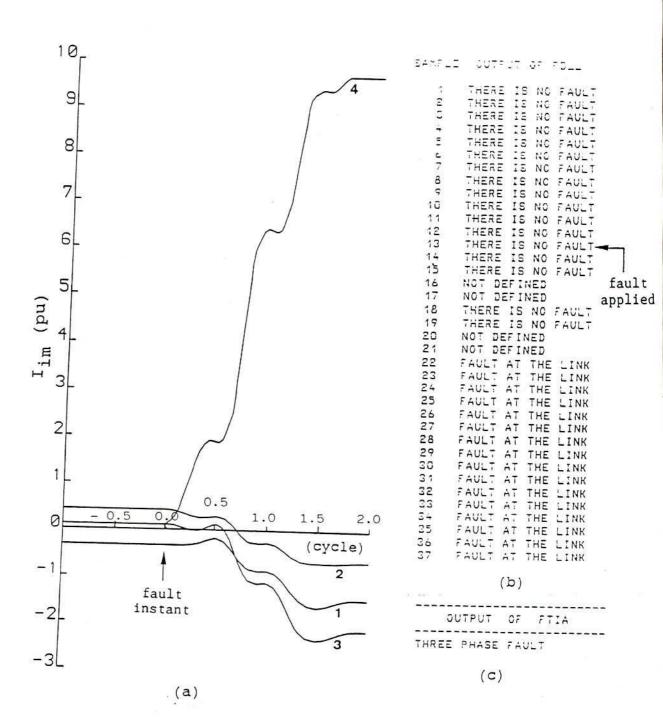


Figure 6.9; a) Behaviour of I_{im} at positions 1, 2, 3 and 4 before and after a three phase fault through 1.0Ω arc resistance at the link with power being imported prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

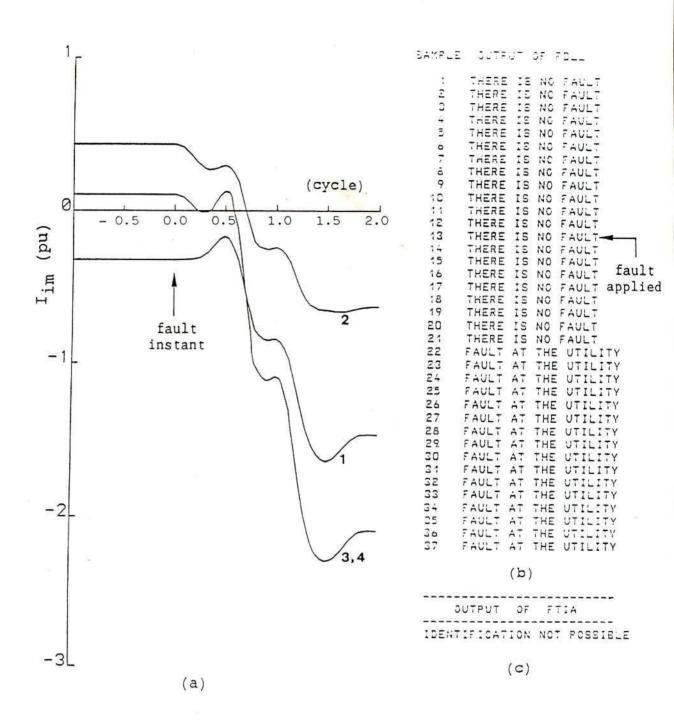


Figure 6.10: a) Behaviour of I_{im} at positions 1, 2, 3, and 4 before and after a three phase fault through 1.00 arc resistance at the utility side with power being imported prior to the fault.

b) Output of FDLL.
c) Output of FTIA.

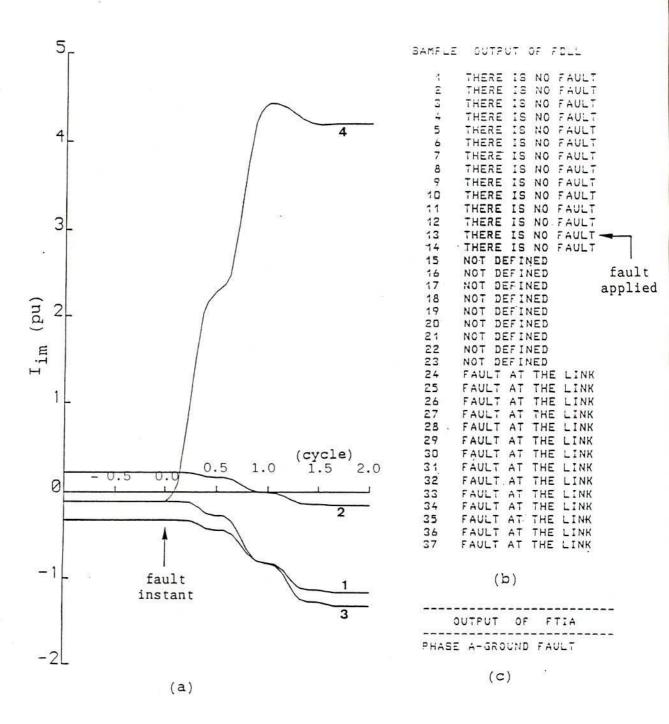


Figure 6.11: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a single line to solid ground fault at the link with 30 MVA generation and 20 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

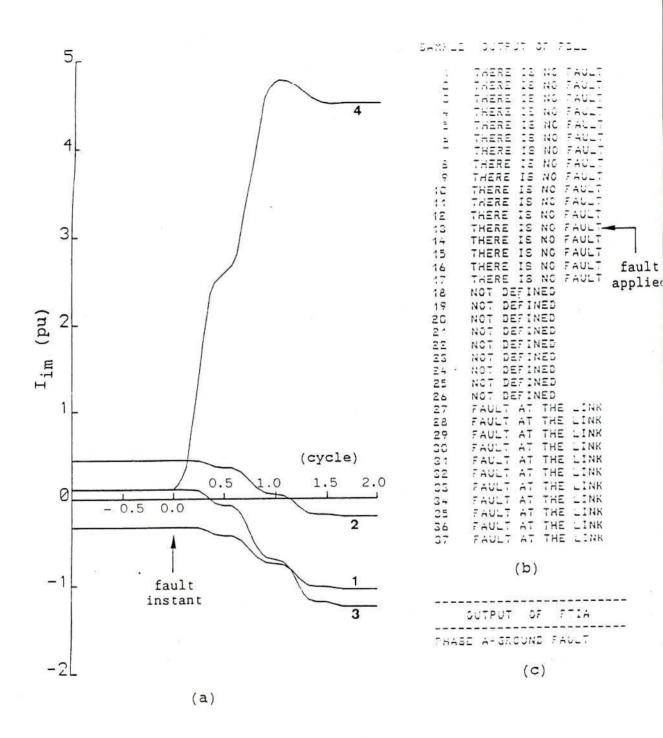


Figure 6.12: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a single line to solid ground fault at the link with 30 MVA generation and 40 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

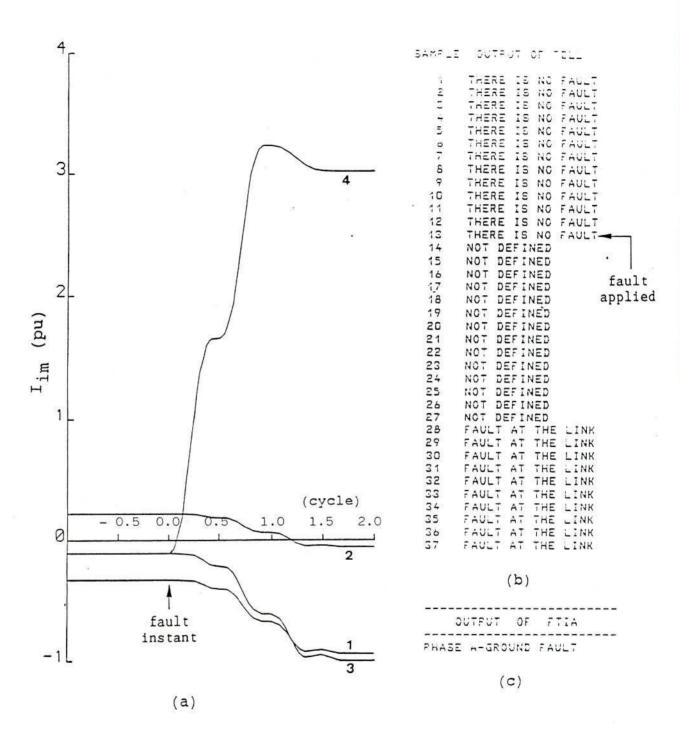


Figure 6.13: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a single line to ground fault through 1.0 Ω arc resistance at the link with 30 MVA generation and 20 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

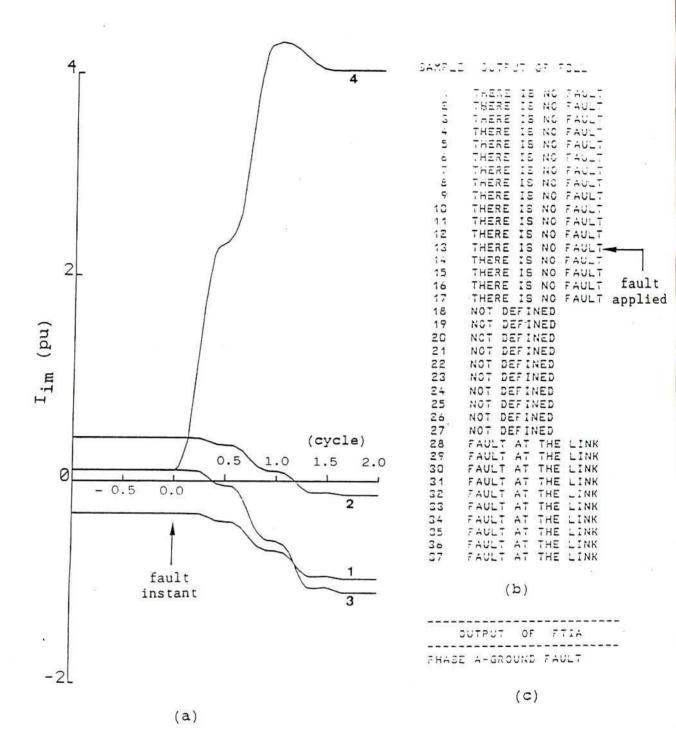


Figure 6.14: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a single line to ground fault through 0.5 α resistance at the link with 30 MVA generation and 40 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

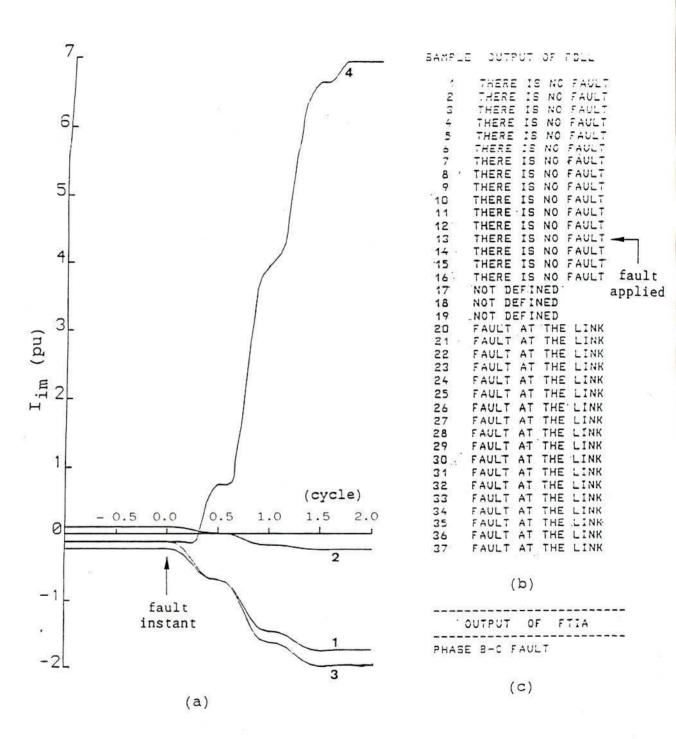


Figure 6.15: a) Behaviour of $I_{\mbox{im}}$ at positions 1, 2, 3 and 4 for a line to line solid fault at the link with 20 MVA generation and 10 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

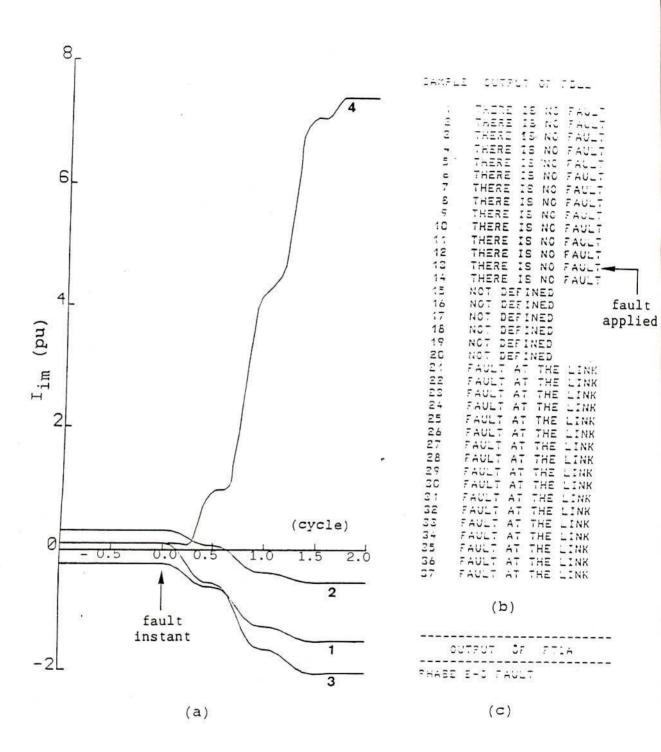


Figure 6.16: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a line to line solid fault at the link with 20 MVA generation and 30 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

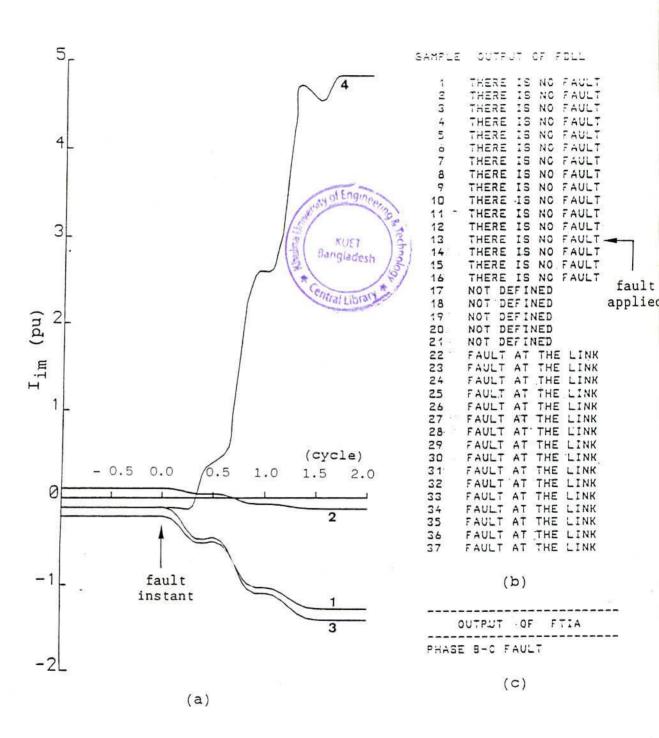


Figure 6.17: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a line to line fault through 2.0 Ω arc resistance at the link with 20 MVA generation and 10 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

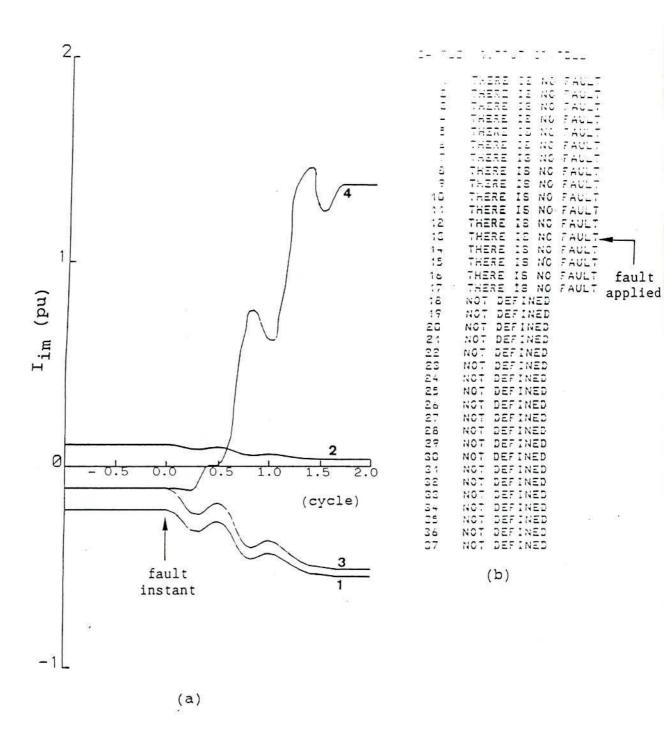


Figure 6.18: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a line to line fault through 6.0 \(\alpha \) arc resistance at the link with 20 MVA generation and 10 MVA motor load prior to the fault.

b) Output of FDLL.

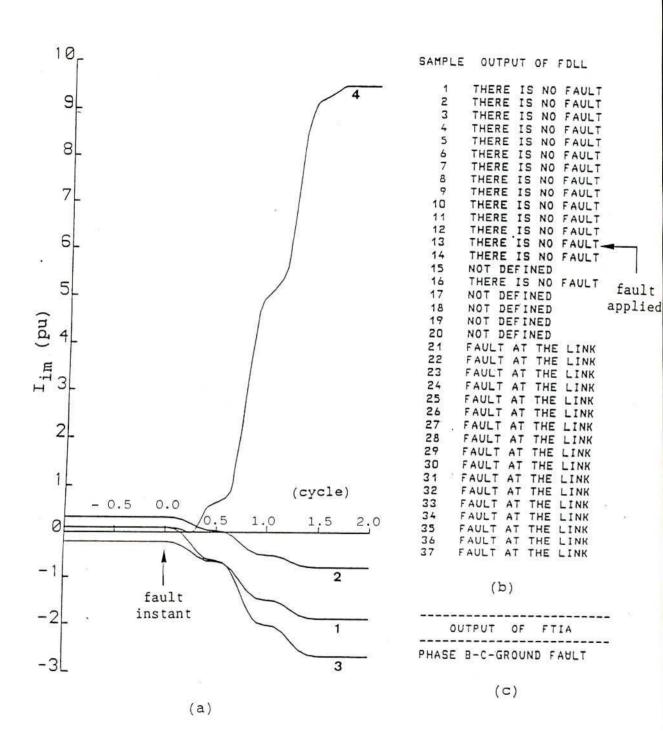


Figure 6.19: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a double line to solid ground fault at the link with 20 MVA generation and 30 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

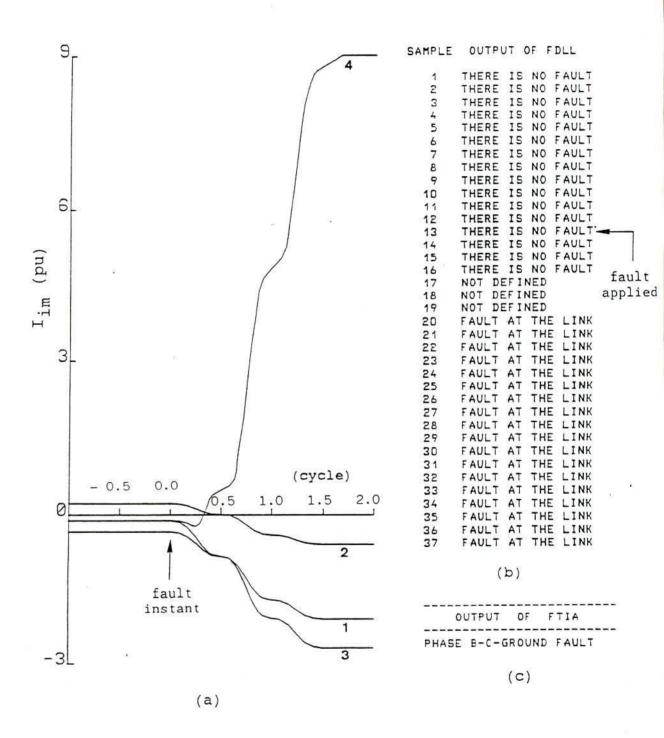


Figure 6.20: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a double line to solid ground fault at the link with 30 MVA generation and 20 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

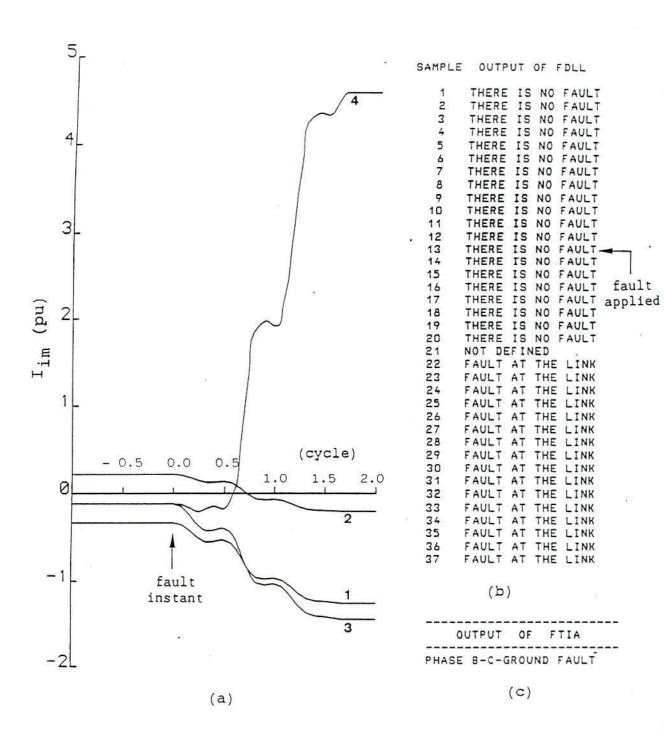


Figure 6.21: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a double line to ground fault through 3.0 α arc resistance at the link with 30 MVA generation and 20 MVA motor load prior to the fault.

- b) Output of FDLL.
- c) Output of FTIA.

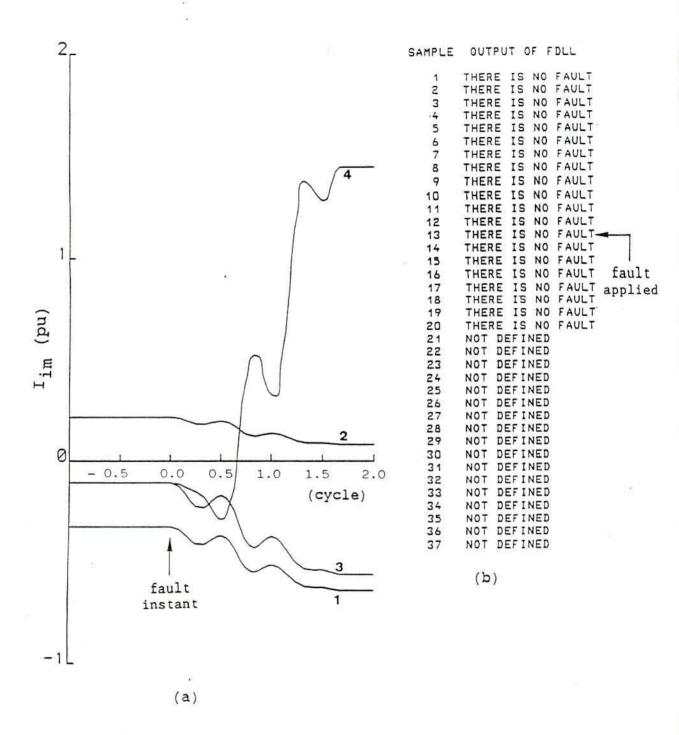


Figure 6.22: a) Behaviour of I_{im} at positions 1, 2, 3 and 4 for a double line to ground fault through 7.0 Ω arc resistance at the link with 30 MVA generation and 20 MVA motor load prior to the fault.

b) Output of FDLL.

CHAPTER SEVEN

CONCLUSION AND FUTURE WORK

7.1 Conclusion

The objectives of this research have been firstly, to develop a microprocessor based technique to detect and locate symmetrical and unsymmetrical faults on the interfacing network of a utility interconnected industrial cogenerator system, secondly, to identify the type of the detected fault.

In order to provide operational flexibility and supply security to such an interconnected industrial cogenerator plant, fault location is regarded as being of prime importance. Current protection practices for this sort of interconnected cogeneration system were reviewed. This helped to conclude that conventional protection schemes are complex and expensive. This highlighted the necessity of developing a simple, cheap and reliable alternative to the conventional scheme.

The problems and limitations of the application of standard IDMT relays for the overcurrent protection of this sort of interconnected system were identified.

A review of digital protection and its various algorithms was undertaken. This provided the basis for a rational choice of algorithm for the proposed new technique.

The basis of the proposed technique was, firstly, the determination of pps current directions at four selected positions on the simulated system and then identification of the combination of these directions which represented the system condition (i.e. either normal operating or fault). It was deduced from the study that the sign of the imaginary part of the fundamental component of pps current could be used as a means to determine the direction of that current with respect to some polarising reference. The pps voltage of the industrial busbar was used as the polarising reference. The sequence of functions of the proposed protection scheme could be summarised as follows: First, phase currents at the selected positions in the system were sampled. The pps currents at those positions were then obtained in sampled form from the phase currents samples at the corresponding positions. Then, these pps currents, containing fundamentals along with other harmonics and dc components, were used in the Fourier filtering algorithm to extract only fundamental components in rectangular form. Signs of imaginary parts of these components were then used to determine the directions of pps currents at the selected positions. Finally, these directions were used in a fault detection and location subroutine, call FDLL, to determine the system condition (i.e. whether the system was under fault or normal operating condition) and the location of any fault. After detecting a fault and locating its position, the type of fault was then determined from off-line analysis of the postfault phase currents at position 3 or position 4, depending on the location of the fault. The analysis of the fault identification was based on identifying the phases carrying the maximum fault currents and checking the

presence of zero sequence current.

A utility interconnected industrial cogeneration system and the associated protection scheme were simulated on a mainframe computer in order to test the performance of the proposed scheme. Both symmetrical and unsymmetrical short circuit faults at different locations on the system were considered. The performance was found to be satisfactory for all kinds of solid and low resistance faults. In fact, three phase, line-to-line and double line-to-ground faults were detected and located well within one cycle following inception of the fault. Single line-to-ground faults were detected within just over one cycle, which is considered to be fast enough for the protection scheme of the type of distribution system under discussion. It was also observed from the tests that solid short circuit faults were detected and located faster than faults with arc resistance, and the detection time became longer with the increase in the fault path resistance. Nevertheless, the fault detection time remained within the period mentioned above. The proposed microprocessor based protection scheme was found to be successful in providing the following functions : differential protection of the interface link and the industrial busbar, overcurrent protection of the motor feeder and reverse power protection of the cogenerator. So, the proposed scheme was expected to be cheaper than its conventional counterpart.

Thus the objectives of the research work outlined in the introductory chapter have been essentially achieved.

It is felt, however, that there is a scope for further investigation

to improve the performance of the scheme for condition of faults with very high arcing (or fault path) resistance. Such faults could not be detected by the scheme thus far developed.

Although the proposed protection scheme was developed and exclusively tested assuming that the system was operating under lagging power factor conditions, the scheme is also applicable to leading power factor conditions.

7.2 <u>Suggestions for future work</u>

As described in chapter 5, fault current contribution from the generator or the motor to a three phase short circuit, in particular, has been considered as asymmetrical, consisting of exponentially decaying a symmetrical ac component and a dc offset. However, no harmonic components have been considered in the simulation of the fault currents. Clearly harmonics could be included in the simulation of fault currents at the selected positions in order to achieve more realistic representations. Saturation of CTs and the corresponding effects on the performance of the protection scheme also needs to be studied.

As mentioned earlier, the proposed scheme successfully detects and locates solid and low resistance faults. If, however, the fault path resistance exceeds a particular limit, which has been presented in table 6:1 of chapter 6, the scheme cannot detect the fault. Further work is required to improve the performance of the scheme under such fault conditions. One possibility would be to use the postfault pps

voltage of bus 1 as the polarising reference to determine the pps current directions under such high resistance faults. In developing the proposed scheme the prefault pps voltage has been used as the polarising reference under all conditions (i.e. both normal operating and fault).

Power system transients caused by power swings and switching are also major areas of concern for any protection scheme. The performance of the proposed scheme should be investigated under such transient conditions, particularly during sudden load changes, motor starting and loss of the generator when the system experiences large voltage variations. This will require a more detailed model of the generator and the motor. In order to keep the scheme stable under such conditions, tripping times may require to be extended.

The next logical step would be to test the performance of the proposed scheme in real-time application. This requires the implementation of the simulated scheme on a microprocessor based hardware system. Careful study of many technical considerations will be required before choosing the signal conditioning part of the hardware system, since this plays an important role on the performance of a digital protection scheme. Some of these considerations are accuracy, linearity requirements and calibration stability. Possible errors resulting from temperature changes, conversion time and power supply stability must also be considered. The nature of the input signal, including relative noise levels, must be fully understood. All these factors should be properly evaluated before choosing a suitable A/D converter to avoid potential errors in the signal

conversion.

The principle on which the proposed scheme is based might also be applicable to an interconnected system having multiple interface links and more than one motor, as shown in Fig. 7.1. However, some modifications are required in the software, particularly in the fault detection and location routines, to accommodate these additions to the system configuration. Further studies are required firstly, to verify the principle of the proposed scheme to a multiple interface links, secondly, to make the proposed scheme flexible so that it can easily accommodate any modification to the system configuration.

The proposed digital scheme is designed to provide primary protections to the system. Should this fail, the scheme must also be capable of providing back-up protection and this requires further study.

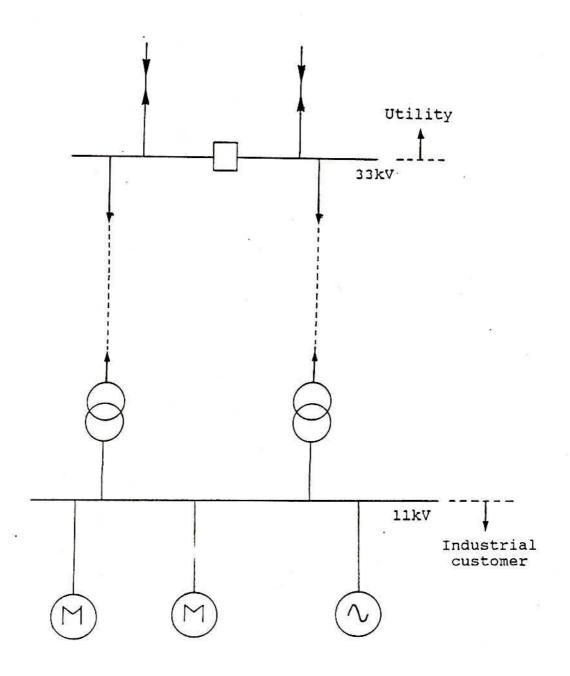


Figure 7.1: Utility interconnected industrial cogeneration system through multiple link.

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APPENDIX-I

DERIVATION OF GENERAL FORMULAE FOR SYMMETRICAL

COMPONENT BUS VOLTAGES AND FAULT CURRENT VECTORS

FOR UNSYMMETRICAL FAULTS

According to Thevenin's theorem the postfault bus voltage, for the case of unsymmetrical faults, can be obtained from the following formula [92].

$$V_{s,bus}^f = V_{s,bus}^0 + Z_{s,bus}^{f}$$
 If s,bus (A.1)

where $\mathbf{v^f}_{s,bus}$, $\mathbf{v^0}_{s,bus}$, $\mathbf{z_{s,bus}}$ and $\mathbf{I^f}_{s,bus}$ are the SC postfault bus voltage vector, SC prefault bus voltage vector, SC bus impedance matrix and SC fault current vector respectively. The definition of these vectors are given in section 5.3.2.2 of chapter 5. Assuming the fault on the qth bus of a n-bus system, the fault current vector $\mathbf{I^f}_{s,bus}$ is given as follows

bus is given as follows

$$I_{s,bus}^{f} = \begin{bmatrix} 0 \\ \vdots \\ -I_{sq}^{f} \end{bmatrix} \longrightarrow qth component$$
(A.2)

When eqn. (A.1) is expanded, it can be expressed in component form, giving a set of n vector equations as follows

$$V^{f}_{s1} = V^{0}_{s1} - Z_{s1q} I^{f}_{sq}$$

$$V^{f}_{sq} = V^{0}_{sq} - Z_{sqq} I^{f}_{sq}$$

$$V^{f}_{sn} = V^{0}_{sn} - Z_{snq} I^{f}_{sq}$$

Before going to proceed further, the relation between the fault current and the faulted bus voltage through fault admittance is considered first. When an unbalanced fault occurs on bus q, the fault results in the fault currents I_{aq}^f , I_{bq}^f and I_{cq}^f in phases a,

b and c respectively. These currents can be expressed by a three element vector as follows

$$\mathbf{I}_{pq}^{f} = \begin{bmatrix} \mathbf{I}_{aq}^{f} \\ \mathbf{I}_{bq}^{f} \\ \mathbf{I}_{cq}^{f} \end{bmatrix}$$
(A.4)

Similarly, phase voltages v^f_{aq} , v^f_{bq} and v^f_{cq} of the faulted bus can be expressed by a three element vector

$$\mathbf{v^f}_{pq} = \begin{bmatrix} \mathbf{v^f}_{aq} \\ \mathbf{v^f}_{bq} \\ \mathbf{v^f}_{cq} \end{bmatrix}$$
(A.5)

The subscripts "p" of vector quantities represent their phase values. If pq and V^f_{pq} are related as follows

$$\mathbf{I}_{pq}^{f} = \mathbf{Y}^{f} \mathbf{V}_{pq}^{f} \tag{A.6}$$

where $\mathbf{Y}^{\mathbf{f}}$ is the fault admittance matrix, the values of which depend on the type of fault. This will be discussed later. The eqn. (A.6) gives the admittance relationship of faulted bus voltage and fault current vectors in actual phase values. In SC values this relation becomes

$$I_{SQ}^{f} = Y_{S}^{f} V_{SQ}^{f} \tag{A.7}$$

where SC fault admittance matrix is

*3

$$\mathbf{Y}^{\mathbf{f}}_{\mathbf{S}} = \mathbf{T}^{-1}\mathbf{Y}^{\mathbf{f}}\mathbf{T} \tag{A.8}$$

The SC transformation matrix is

$$T = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix}$$
 (A.9)

where $a = 1/120^{\circ}$ and $a^2 = 1/240^{\circ}$.

Now substituting eqn. (A.7) into the qth eqn. (A.3), we get

$$\mathbf{v}_{sq}^{f} = \mathbf{v}_{sq}^{0} - \mathbf{z}_{sqq} \mathbf{y}_{s}^{f} \mathbf{v}_{sq}^{f} \tag{A.10}$$

Solving this equation for the qth bus postfault voltage vector, $\mathbf{v^f}_{\text{sq}}, \text{ we obtain}$

$$V_{SQ}^{f} = (I + Z_{SQQ} Y_{S}^{f})^{-1} V_{SQ}^{0}$$
 (A.11)

where I is the identity matrix.

Substituting eqn. (A.11) into eqn. (A.7), the fault current vector is obtained as follows

$$I_{sq}^{f} = Y_{s}^{f} V_{sq}^{f}$$

$$= Y_{s}^{f} (I + Z_{sqq} Y_{s}^{f})^{-1} V_{sq}^{0}$$
(A.12)

Now it is possible to obtain the postfault voltages at other buses by substituting eqn. (A.12) into eqn. (A.3)

$$v^{f}_{si} = v^{0}_{si} - z_{siq} I^{f}_{sq}$$

= $v^{0}_{si} - z_{siq} Y^{f}_{s} (I + z_{sqq} Y^{f}_{s})^{-1} V^{0}_{sq} \quad i \neq q$ (A.13)

Before proceeding further to apply eqns. (A.11) to (A.13) for different unbalanced faults, a brief description of computation procedure of SC fault admittance matrix, $\mathbf{Y}^{\mathrm{f}}_{\mathrm{S}}$, is presented first. Consider a general unbalanced case, shown in Fig. A.1.

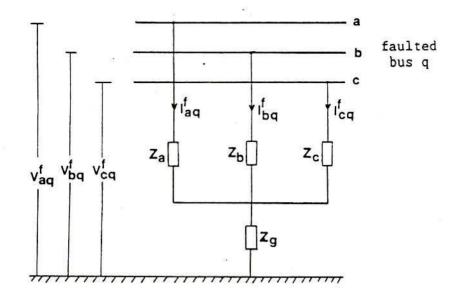


Fig. A.1: A general unbalanced fault case where $z_a \neq z_b \neq z_c \neq z_g$.

By assigning proper values to the impedances, any fault case can be created. For example, by setting

$$Z_a = Z_g = 0$$
 i.e. $Y_a = Y_g = \infty$
 $Z_b = Z_c = \infty$ i.e. $Y_a = Y_b = 0$

a solid line-to-ground short circuit on phase "a" is created. By applying nodal analysis in Fig. A.1, the relation between phase currents and voltages in admittance form are obtained as follows

$$\begin{bmatrix} \mathbf{I}^{f}_{aq} \\ \mathbf{I}^{f}_{bq} \\ \mathbf{I}^{f}_{cq} \end{bmatrix} = \frac{1}{\mathbf{Y}_{a} + \mathbf{Y}_{b} + \mathbf{Y}_{c} + \mathbf{Y}_{g}} \times \begin{bmatrix} \mathbf{Y}_{a} + \mathbf{Y}_{b} + \mathbf{Y}_{c} & -\mathbf{Y}_{a}\mathbf{Y}_{b} & -\mathbf{Y}_{a}\mathbf{Y}_{c} \\ -\mathbf{Y}_{a}\mathbf{Y}_{b} & \mathbf{Y}_{b}(\mathbf{Y}_{g} + \mathbf{Y}_{a} + \mathbf{Y}_{c}) & -\mathbf{Y}_{b}\mathbf{Y}_{c} \\ -\mathbf{Y}_{a}\mathbf{Y}_{c} & -\mathbf{Y}_{b}\mathbf{Y}_{c} & \mathbf{Y}_{c}(\mathbf{Y}_{g} + \mathbf{Y}_{a} + \mathbf{Y}_{b}) \end{bmatrix} \begin{bmatrix} \mathbf{V}^{f}_{aq} \\ \mathbf{V}^{f}_{bq} \\ \mathbf{V}^{f}_{cq} \end{bmatrix}$$

(A.14)

Substituting this fault admittance matrix, $\mathbf{Y}^{\mathbf{f}}$, in eqn. (A.8), the SC fault admittance matrix, $\mathbf{Y}^{\mathbf{f}}_{\mathbf{S}}$, can be obtained as follows

$$Y^{f}_{s} = \frac{1}{Y_{a} + Y_{b} + Y_{c} + Y_{g}} \times \begin{bmatrix} (1/3)Y_{g}(Y_{a} + a^{2}Y_{b} + aY_{c}) & (1/3)Y_{g}(Y_{a} + a^{2}Y_{b} + aY_{c}) & (1/3)Y_{g}(Y_{a} + aY_{b} + a^{2}Y_{c}) \\ + (Y_{a}Y_{b} + Y_{b}Y_{c} + Y_{c}Y_{a}) & -(Y_{b}Y_{c} + aY_{a}Y_{b} + a^{2}Y_{a}Y_{c}) & (1/3)Y_{g}(Y_{a} + aY_{b} + a^{2}Y_{c}) \\ -(Y_{b}Y_{c} + aY_{b} + aY_{a}Y_{c}) & (1/3)Y_{g}(Y_{a} + Y_{b} + Y_{c}) & (1/3)Y_{g}(Y_{a} + a^{2}Y_{b} + aY_{c}) \\ -(Y_{b}Y_{c} + a^{2}Y_{a}Y_{b} + aY_{a}Y_{c}) & +(Y_{a}Y_{b} + Y_{b}Y_{c} + Y_{c}Y_{a}) & (1/3)Y_{g}(Y_{a} + a^{2}Y_{b} + aY_{c}) \\ -(1/3)Y_{g}(Y_{a} + a^{2}Y_{b} + aY_{c}) & (1/3)Y_{g}(Y_{a} + aY_{b} + a^{2}Y_{c}) & (1/3)Y_{g}(Y_{a} + Y_{b} + Y_{c}) \end{bmatrix}$$

(A.15)

Single line-to-ground short circuit

A single line-to-ground short circuit at qth bus is shown in the following Fig. A.2.

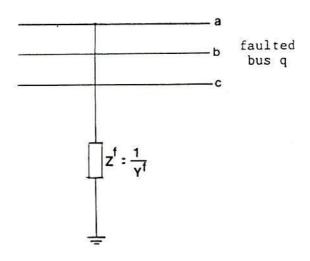


Fig. A.2: The single line-to-ground fault case.

This case is obtained by setting

$$Z_b = Z_c = \infty$$
, i.e. $Y_b = Y_c = 0$
 $Z_g = 0$, i.e. $Y_g = \infty$
 $Z_a = Z^f$, i.e. $Y_a = 1/Z^f = Y^f$

Substituting these admittance values into eqn. (A.15), we obtain

$$\mathbf{Y}^{f}_{S} = \frac{\mathbf{Y}^{f}}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$
 (A.16)

By substituting eqn. (A.16) into eqn. (A.11), the postfault voltage vector at the faulted bus is evaluated as follows

$$\mathbf{v^f}_{sq} = \begin{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} \mathbf{z_{+qq}} & 0 & 0 \\ 0 & \mathbf{z_{-qq}} & 0 \\ 0 & 0 & \mathbf{z_{0qq}} \end{bmatrix} & \mathbf{v^f}_{q} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} & \begin{bmatrix} \mathbf{v^0_q} \\ 0 \\ 0 \end{bmatrix}$$

By performing the matrix operation, the vector equation becomes

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{1 + (\mathbf{Y}^{f}/3)(z_{+qq} + z_{-qq} + z_{0qq})} \begin{bmatrix} 1 + (\mathbf{Y}^{f}/3)(z_{-qq} + z_{0qq}) \\ - (\mathbf{Y}^{f}/3)z_{-qq} \\ - (\mathbf{Y}^{f}/3)z_{0qq} \end{bmatrix}$$
(A.17)

By substituting eqn. (A.17) into eqn. (A.12), the short circuit current at the faulted bus is obtained

$$\mathbf{I}_{sq}^{f} = \mathbf{Y}_{s}^{f} \mathbf{V}_{sq}^{f} = \frac{(\mathbf{Y}^{f/3})\mathbf{V}_{q}^{0}}{1 + (\mathbf{Y}^{f/3})(\mathbf{z}_{+qq}^{+z} - qq^{+z} - qq^{+z} - qq^{+z})} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$
(A.18)

Then substituting $\mathbf{I_{sq}^f}$, defined by eqn. (A.18), into eqn. (A.13), the postfault voltages vector of the buses other than the faulted one is obtained

$$\mathbf{v^{f}_{si}} = \mathbf{v^{0}_{si}} - \mathbf{z_{siq}} \mathbf{I^{f}_{sq}}$$

$$= \begin{bmatrix} \mathbf{v^{0}_{i}} \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} \mathbf{z_{+iq}} & 0 & 0 \\ 0 & \mathbf{z_{-iq}} & 0 \\ 0 & 0 & \mathbf{z_{0iq}} \end{bmatrix} \frac{(\mathbf{Y^{f/3}}) \mathbf{v^{0}_{q}}}{1 + (\mathbf{Y^{f/3}}) (\mathbf{z_{+qq^{+z}-qq^{+z}0qq}})} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

After matrix operation this equation is reduced to

$$\mathbf{v}^{f}_{si} = \begin{bmatrix} v^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{(Y^{f}/3)V^{0}_{q}}{1 + (Y^{f}/3)(z_{+qq} + z_{-qq} + z_{0qq})} \begin{bmatrix} z_{+iq} \\ z_{-iq} \\ z_{0q} \end{bmatrix} \quad i \neq q \quad (A.19)$$

For solid short circuit, $Y^f = \infty$. Then eqns. (A.17) to (A.19) are reduced to the following forms

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{\mathbf{z}_{+qq}^{+z} - qq^{+z} \cdot 0qq} \begin{bmatrix} \mathbf{z}_{-qq}^{+z} \cdot 0qq \\ -\mathbf{z}_{-qq} \\ -\mathbf{z}_{0qq} \end{bmatrix}$$
(A.20)

$$\mathbf{I}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{\mathbf{z}_{+qq}^{+z} - qq^{+z} 0 q q} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$
 (A.21)

$$\mathbf{v}^{\mathbf{f}}_{\mathbf{S}i} = \begin{bmatrix} \mathbf{v}^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{\mathbf{v}^{0}_{q}}{\mathbf{z}_{+qq}^{+z} - qq^{+z} 0 qq} \begin{bmatrix} \mathbf{z}_{+iq} \\ \mathbf{z}_{-iq} \\ \mathbf{z}_{0iq} \end{bmatrix} \qquad i \neq q \qquad (A.22)$$

Line-to-line short circuit

A line-to-line short circuit at the qth bus is shown in the following Fig. A.3.

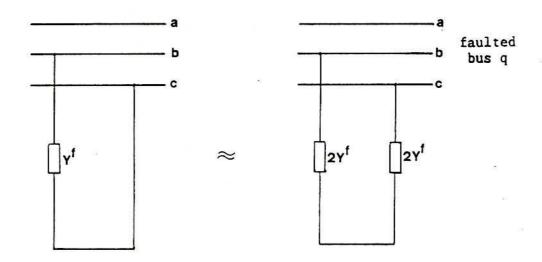


Fig. A.3: The line-to-line short circuit case.

This case is obtained by setting

$$Z_a = \infty$$
 i.e. $Y_a = 0$
 $Z_g = \infty$ i.e. $Y_g = 0$
 $Y_b = Y_c = 2Y^f$

By substituting the values of Y_a , Y_b , Y_c and Y_g in eqn. (A.15), we get

$$\mathbf{Y}_{s}^{f} = \mathbf{Y}^{f} \begin{bmatrix} 1 & -1 & 0 \\ -1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$
 (A.23)

By substituting the values of Y_s^f , I, Z_{sqq} and V_{sq}^0 in eqn. (A.11), the voltage vector at the faulted bus can be derived as follows

$$\mathbf{v^{f}}_{sq} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} z_{+qq} & 0 & 0 \\ 0 & z_{-qq} & 0 \\ 0 & 0 & z_{0qq} \end{bmatrix} \mathbf{v^{f}} \begin{bmatrix} 1 & -1 & 0 \\ -1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} v^{0}_{q} \\ 0 \\ 0 \end{bmatrix}$$

$$= \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} \mathbf{v^{f}}_{z_{+qq}} & -\mathbf{v^{f}}_{z_{+qq}} & 0 \\ -\mathbf{v^{f}}_{z_{-qq}} & \mathbf{v^{f}}_{z_{-qq}} & 0 \\ 0 & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} v^{0}_{q} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} 1 + \mathbf{v^{f}}_{z_{+qq}} & -\mathbf{v^{f}}_{z_{+qq}} & 0 \\ -\mathbf{v^{f}}_{z_{+qq}} & \mathbf{v^{f}}_{z_{-qq}} & 0 \\ 0 & 0 & 0 \end{bmatrix}^{-1} \begin{bmatrix} v^{0}_{q} \\ 0 \\ 0 \end{bmatrix}$$

$$= \begin{bmatrix} 1 + Y^{f}z_{+qq} & -Y^{f}z_{+qq} & 0 \\ -Y^{f}z_{-qq} & 1 + Y^{f}z_{-qq} & 0 \\ 0 & 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V^{0}_{q} \\ 0 \\ 0 \end{bmatrix}$$

After inverting the matrix, the above equation becomes

$$\mathbf{v^f}_{sq} = \frac{1}{1 + \mathbf{v^f}(z_{+qq} + z_{-qq})} \begin{bmatrix} 1 + \mathbf{v^f}_{z_{-qq}} & \mathbf{v^f}_{z_{+qq}} & 0 \\ \mathbf{v^f}_{z_{-qq}} & 1 + \mathbf{v^f}_{z_{+qq}} & 0 \\ 0 & 0 & 1 + \mathbf{v^f}(z_{+qq} + z_{-qq}) \end{bmatrix} \begin{bmatrix} \mathbf{v^0}_q \\ 0 \\ 0 \end{bmatrix}$$

Finally this equation becomes

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{1 + \mathbf{v}^{f}(z_{+qq} + z_{-qq})} \begin{bmatrix} 1 + \mathbf{v}^{f}z_{-qq} \\ \mathbf{v}^{f}z_{-qq} \end{bmatrix}$$
(A.24)

Substituting eqn. (A.24) into eqn. (A.12), the fault current vector at the faulted bus is obtained as follows

$$\mathbf{If}_{sq} = \mathbf{Y}^{f} \begin{bmatrix} 1 & -1 & 0 \\ -1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \frac{\mathbf{V}_{q}^{0}}{\mathbf{I} + \mathbf{Y}^{f}(\mathbf{z}_{+qq} + \mathbf{z}_{-qq})} \begin{bmatrix} \mathbf{I} + \mathbf{Y}^{f}\mathbf{z}_{-qq} \\ \mathbf{Y}^{f}\mathbf{z}_{-qq} \\ 0 \end{bmatrix}$$

After simplifying, the last equation becomes

L

$$I_{sq}^{f} = \frac{Y_{qq}^{f} Q_{q}^{0}}{1 + Y_{qq}^{f} Z_{qq}^{+} Z_{qq}^{0}} \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix}$$
(A.25)

Substituting eqn. (A.25) into eqn. (A.13), the voltage vector at the buses other than the faulted one is obtained as follows

$$\mathbf{v^{f}_{si}} = \begin{bmatrix} v^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} z_{+qq} & 0 & 0 \\ 0 & z_{-iq} & 0 \\ 0 & 0 & z_{0iq} \end{bmatrix} \frac{y^{f}v^{0}_{q}}{1 + y^{f}(z_{+qq} + z_{-qq})} \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix}$$

which can be reduced to the following form

$$\mathbf{v^f_{si}} = \begin{bmatrix} \mathbf{v^0_i} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} - \frac{\mathbf{v^f v^0_q}}{\mathbf{1 + \mathbf{v^f}(z_{+qq} + z_{-qq})}} \begin{bmatrix} z_{+iq} \\ -z_{-iq} \\ \mathbf{0} \end{bmatrix} \qquad i \neq q \qquad (A.26)$$

When the short circuit is solid, i.e. $Y^f = \infty$, then eqns. (A.24) to (A.26) are reduced as follows

$$\mathbf{v^f}_{\mathbf{sq}} = \frac{\mathbf{v^0}_{\mathbf{q}}}{\mathbf{z}_{+\mathbf{qq}} + \mathbf{z}_{-\mathbf{qq}}} \begin{bmatrix} \mathbf{z}_{-\mathbf{qq}} \\ \mathbf{z}_{-\mathbf{qq}} \\ 0 \end{bmatrix}$$
(A.27)

$$\mathbf{I_{sq}} = \frac{\mathbf{v_q}}{\mathbf{z_{+qq}} + \mathbf{z_{-qq}}} \begin{bmatrix} 1\\-1\\0 \end{bmatrix}$$
 (A.28)

$$\mathbf{v^f}_{si} = \begin{bmatrix} \mathbf{v^0}_i \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} - \frac{\mathbf{v^0}_q}{\mathbf{z_{+qq} + z_{-qq}}} \begin{bmatrix} \mathbf{z_{+iq}} \\ -\mathbf{z_{-iq}} \\ \mathbf{0} \end{bmatrix} \qquad i \neq q \qquad (A.29)$$

Double line-to-ground short circuit

A double line-to-ground short circuit at the qth bus is shown in the following Fig. A.4.

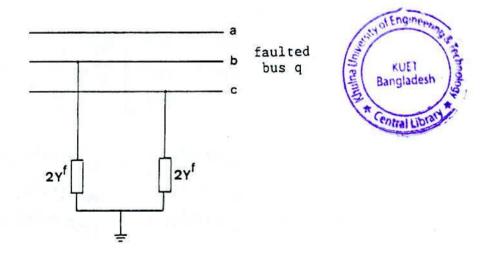


Fig. A.4: The double line-to-ground short circuit.

$$v_{sq}^f =$$

$$\frac{v^{0}_{q}}{1+(4Y^{f}/3)(z_{+qq}^{+z}-qq^{+z}0qq)^{+}(4Y^{f2}/3)(z_{+qq}^{z}-qq^{+z}-qq^{z}0qq^{+z}0qq^{z}^{-t}qq)}^{\star}$$

$$\begin{bmatrix} 1 + (4Y^{f}/3)z_{0qq} + (4Y^{f}/3)z_{-qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \\ (2Y^{f}/3)z_{-qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \\ (2Y^{f}/3)z_{0qq} + (4Y^{f2}/3)z_{0qq}z_{-qq} \end{bmatrix}$$
(A.31)

Now by substituting $\mathbf{Y}^f_{\ S}$ and $\mathbf{V}^f_{\ Sq}$ into eqn. (A.12), the current vector at the faulted bus is obtained as follows

$$\frac{(2Y^{f}/3) \ V^{0}_{q}}{1+(4Y^{f}/3)(z_{+qq}^{+z}-qq^{+z}0qq)+(4Y^{f2}/3)(z_{+qq}^{z}-qq^{+z}-qq^{z}0qq^{+z}0qq^{z}+qq)} \times \\ \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 1+(4Y^{f}/3)z_{0qq}^{+}+(4Y^{f}/3)z_{-qq}^{+}+(4Y^{f2}/3)z_{0qq}^{z}-qq \\ (2Y^{f}/3)z_{-qq}^{+}+(4Y^{f2}/3)z_{0qq}^{z}-qq \\ (2Y^{f}/3)z_{0qq}^{+}+(4Y^{f2}/3)z_{0qq}^{z}-qq \end{bmatrix}$$

After simplification,

$$\mathbf{I}^{\mathsf{f}}_{\mathsf{sq}} =$$

$$\frac{(2Y^{f}/3) V^{0}_{q}}{1+(4Y^{f}/3)(z_{+qq}+z_{-qq}+z_{0qq})+(4Y^{f2}/3)(z_{+qq}z_{-qq}+z_{-qq}z_{0qq}+z_{0qq}z_{+qq})}{2+2Y^{f}z_{0qq}+2Y^{f}z_{-qq}}$$

$$-1-2Y^{f}z_{0qq}$$

$$-1-2Y^{f}z_{-qq}$$

$$-1-2Y^{f}z_{-qq}$$
(A.32)

Inserting $\mathbf{I_{sq}^f}$ into eqn. (A.13) the voltage vector at buses other than the faulted one is obtained as follows

$$\mathbf{v^f}_{si} = \begin{bmatrix} \mathbf{v^0}_{si} \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} \mathbf{z_{+iq}} & 0 & 0 \\ 0 & \mathbf{z_{-iq}} & 0 \\ 0 & 0 & \mathbf{z_{0iq}} \end{bmatrix} \begin{bmatrix} \mathbf{I^f}_{sq} \end{bmatrix}$$

After simplification, we obtain

$$\mathbf{v}^{\mathbf{f}}_{si} = \begin{bmatrix} v^{0}_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{(2Y^{f}/3) \ V^{0}_{q}}{1 + (4Y^{f}/3)(z_{+qq} + z_{-qq} + z_{0qq}) + (4Y^{f2}/3)(z_{+qq} z_{-qq} + z_{-qq} z_{0qq} + z_{0qq} z_{+qq})}$$

$$\begin{bmatrix} z_{+iq} & (2+2Y^{f}(z_{0qq}+z_{-qq})) \\ z_{-iq} & (-1-2Y^{f}z_{0qq}) \\ z_{0iq} & (-1-2Y^{f}z_{-qq}) \end{bmatrix} \qquad i \neq q \qquad (A.33)$$

Assuming solid short circuit fault, i.e. $Y^f = \infty$, eqns. (A.31) to (A.33) reduce to the following form

$$\mathbf{v}^{f}_{sq} = \frac{\mathbf{v}^{0}_{q}}{\mathbf{z}_{+qq}\mathbf{z}_{-qq} + \mathbf{z}_{-qq}\mathbf{z}_{0qq} + \mathbf{z}_{0qq}\mathbf{z}_{+qq}} \begin{bmatrix} \mathbf{z}_{0qq} & \mathbf{z}_{-qq} \\ \mathbf{z}_{0qq} & \mathbf{z}_{-qq} \\ \mathbf{z}_{0qq} & \mathbf{z}_{-qq} \end{bmatrix}$$
(A.34)

$$\mathbf{I}^{f}_{sq} = \frac{v^{0}_{q}}{z_{+qq}^{z}_{-qq} + z_{-qq}^{z}_{0qq} + z_{0qq}^{z}_{+qq}} \begin{bmatrix} z_{0qq}^{+z}_{-qq} \\ -z_{0qq} \\ -z_{-qq} \end{bmatrix}$$
(A.35)

$$\mathbf{v^f_{si}} = \begin{bmatrix} v^0_{i} \\ 0 \\ 0 \end{bmatrix} - \frac{v^0_{q}}{z_{+qq}^z - qq^{+z} - qq^z 0 qq^{+z} 0 qq^z + qq} \begin{bmatrix} z_{+iq}(z_{0qq}^{+z} - qq) \\ -z_{-iq}z_{0qq} \\ -z_{0iq}z_{-qq} \end{bmatrix}$$
(A.36)
$$for \quad i \neq q$$