Modeling and Simulation of CNT based tunnel FET

by

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Engineering in the Department of Electrical and Electronic Engineering

KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY
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February, 2017

Declaration

This is to certify that the thesis work entitled "**Modeling and Simulation of CNT based tunnel FET**" has been carried out by Md. Shamim Sarker in the Department of Electrical and Electronic Engineering, Khulna University of Engineering & Technology, Khulna, Bangladesh. The above thesis work or any part of this work has not been submitted anywhere for the award of any degree or diploma.

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Approval

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Abstract

MOSFETs are commonly used in high speed integrated circuits and are yielding smaller, faster and more functions at lower cost. Various problems exist with scaling of MOSFET devices including short channel effects such as drain induced barrier lowering, parasitic capacitance, velocity saturation e.t.c. which limit the performances of MOSFETs. Scaling issues of MOSFET devices lead to lower ON to OFF current ratio limited by temperature constrained 60mV/dec subthreshold swing. A new type of device called "Tunnel FET" is predicted to overcome these difficulties. TFET can beat 60mV/dec subthreshold swing of MOSFET. In tunnel FET, carriers are transported by band to band tunneling and its OFF current is very low. This makes it ideal candidate for ultra-low power electronics. Since the tunneling FET relies on the band to band tunneling mechanism, the TFET using conventional material like silicon have very low on state current due to its large indirect band gap. Carbon nanotube has a potential to be the appropriate channel material in this new technology due to its unique quasi one dimensional property such as high electron mobility and high Fermi velocity. This new type of device requires rigorous analysis with various structures and parameters and hence to find out optimum condition for practical device realization. In this thesis we proposed and simulated two double gate CNT TFET structures: (i) Oxide only over the channel (OXOC structure) (ii) Oxide extended over source to drain (OXESD structure), taking into account of different device parameters including dielectric strength and thickness of gate oxide materials, channel length, doping concentration and gate underlap. Here the transfer characteristics, on/off current (I_{ON}/I_{OFF}) ratio and subthreshold slope of the device are studied using Non Equilibrium Greens Function (NEGF) formalism in tight binding frameworks. The results are obtained by solving the NEGF and Poisson's equation self-consistently in NanoTCAD ViDES environment and found that OXOC structure shows significantly better performance than OXESD structure in all cases having highest ON current of 4046 μA/μm and subthreshold swing of 10.19 mV/decade so far reported for CNT TFET. The results obtained from the simulation for both of the device structures are explained by the energy band diagram and electric field. The presented study is expected to be useful for realizing the switching device capable of operating at high speed and low power applications.

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Md. Shamim Sarker

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Abbreviation

MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
TFET	-	Tunneling Field Effect Transistor
MOSCAP	-	Metal Oxide Semiconductor Capacitor
DG	-	Double Gate
T.G	-	Top Gate
B.G	-	Bottom Gate
ITRS	-	International Technology Roadmap of Semiconductor
EOT	-	Equivalent Oxide Thickness
T_{OX}	-	Oxide Thickness
TB	-	Tight Binding
NEGF	-	Non-equilibrium Green Function
CB	-	Conduction Band
VB	-	Valance Band
BTBT	-	Band to Band Tunneling
CMOS	-	Complementary Metal Oxide Semiconductor
WKB	-	Wentzel–Kramers–Brillouin

Dedicated to My Family

My Heaven .....

Chapter 1 : INTRODUCTION

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Chapter Outlines

- **Background of the thesis**
- **Advent of Tunnel FET**
- **Challenges and Scopes in TFET**
- **Objectives of the thesis**
- **Thesis Layout**

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1.1 Background of the thesis

In recent years extensive research interest has been growing on tunnel FET due to its application in high speed low power devices. In order to understand why tunnel tunnel FET is interesting instead of conventional MOSFETs, we need to begin with an explanation of Dennard's scaling rules.

In 1974, R. Dennard, et al. published an article which has become very famous in the semiconductor device community. In his article he pointed out how to scale down a MOSFET, while keeping the electric fields inside the device unchanged [1]. He recommended that all device dimensions be scaled by $1/\kappa$, while the doping of the source and drain regions should increase by a factor of κ. Applied voltages should also be scaled by $1/\kappa$. These rules have been roughly followed ever since, until rather recently.

The reason of the failure of Dennard's scaling rule at current time is explained in Fig.1.1. Here it is seen that when the device scaling goes from 1.4 μm node to 65 nm node, the supply voltage V_{DD} is decreased by about 80% of its original value but the threshold voltage V_T went down to approximately only half of its staring value. That is the reduction of threshold voltage didn't happen naturally as it is required by Dennard's scaling rule. It had to come about in other ways, such as changing the doping of the channel region under the gate. Since the electric fields inside a MOSFET stay nearly constant when the scaling rules are followed correctly, the threshold voltage stays nearly constant as well, unless other changes are made.

The most important consequences of inconsistence scaling of supply voltage and threshold voltage is the reduction of gate overdrive, shown in Fig. 1.1. The reduction of gate overdrive reduces the ON current, which in turns affects the device performance e.g. I_{ON}/I_{OFF} ratio and dynamic speed C_gV_{DD}/I_{ON} negatively. There are two possible solutions to this problem to get a higher gate overdrive that is either V_{DD} can be kept higher than it should be for constant

electric field scaling or V_T can be scaled down more aggressively. The advantages and flaws of both options will be discussed later.

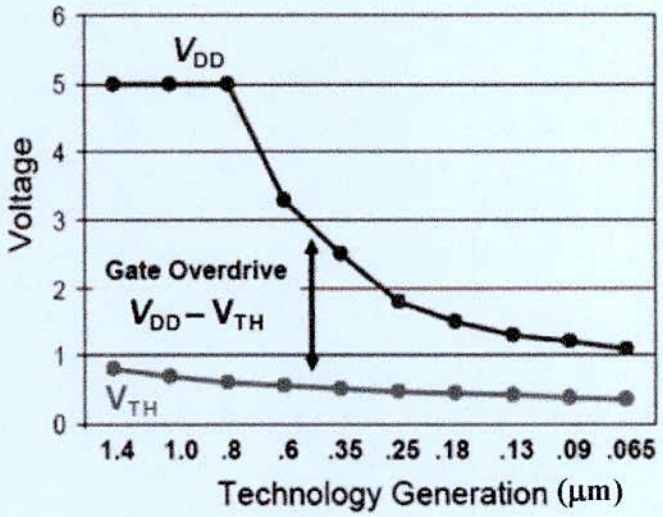

Figure 1.1: Scaling trends of supply voltage and threshold voltage with technology node. Scaling of threshold voltage didn't happen consistently with supply voltage [2]

Fig. 1.2 shows the formerly followed scaling trends of $1/\kappa = 0.7$ every 2 or 3 years (red bold solid and red bold dashed lines for reference) at the top of the figure along with the current trends. Here it is seen that this scaling rule is no longer followed for V_{DD}. The V_{DD} scaling has been slowed down significantly in order to maintain an acceptable level of gate overdrive. Here consider some cases:

(i) Scaling down of V_{DD}: If the supply voltage decreases along with the device dimension, then the power density $I_{ON}V_{DD} / A$ (on-current times supply voltage divided by surface area) remains constants. As a result the energy needed to drive the chip and the heat produced by the chip remains constant. Thus the size of heat sink can't be scaled down which actually determines the chip size. That means the chip size does not decreases, rather more complexity and functionality is added with each generation.

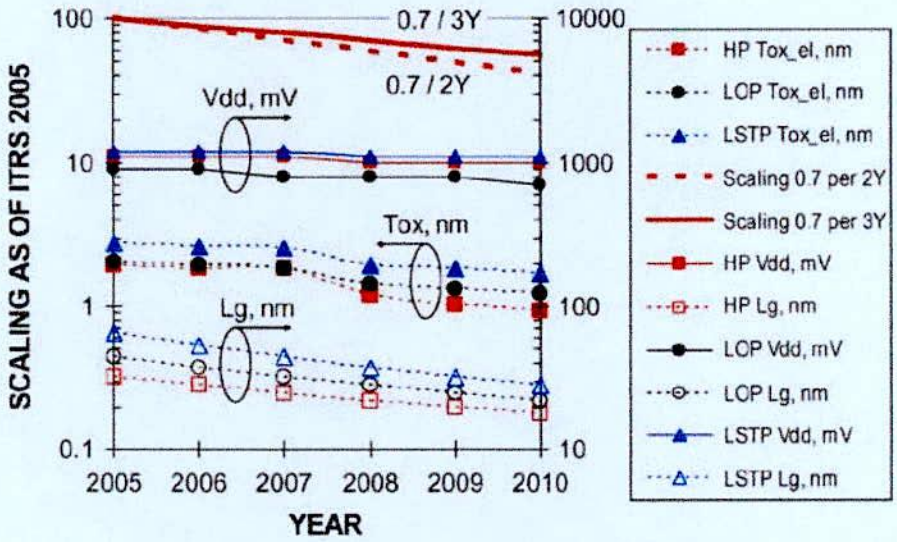

Figure 1.2: Current scaling trends showing that T_{OX} and L_g follows the scaling rule but V_{DD} does not [3].

If V_{DD} doesn't scale down with scaling of device dimension, the power density will increase instead. For each MOSFET, the dynamic and static power consumption can be expressed as [4]

$$P_{dynamic} = fC_L V_{DD}^2 \quad (1.1.1)$$

where f is the frequency and C_L is the total switched capacitive load, and

$$P_{static} = I_{leak} V_{DD} \quad (1.1.2)$$

where I_{leak} is the sum of leakage currents in the device when the MOSFET is in the off state

If V_{DD} does not decrease, and yet device dimension decreases, and more devices are added to a chip such that chip size is not significantly reduced, then it can be expected that power consumption will rise considerably. The current trend of increasing power is illustrated in Fig. 1.3.

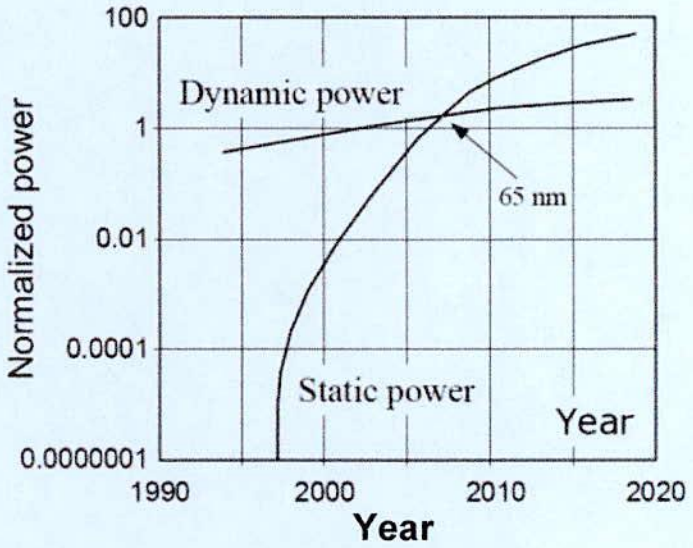

Figure 1.3: Trends of dynamic and static CMOS power, showing that static power consumption has become a greater problem than dynamic power consumption [8]

(ii) Scaling down of V_T: The discussion up until now has not explained why static power would be increasing much faster than dynamic power, and that comes back to the second option for keeping a high gate overdrive: scaling down V_T.

One of the most important characteristics of conventional MOSFET is its temperature constrained subthreshold slope limit of 60 mV/dec at room temperature when, the transfer characteristics of the device is plotted in log-linear scale. That means once a device is fully optimized the most abrupt possible turn-on with gate voltage that is characterized by subthreshold slope $S = dV_{GS}/d(\log I_{DS})$ has hit its limit of 60 mV/decade at room temperature. Thus we have a fixed threshold voltage. The only way to reduce the threshold voltage V_T is to shift the I_D-V_{GS} curve horizontally to the left shown in Fig. 1.4. If we want to shift the curve 60mV/decade we will have to pay it in cost of one decade increase of OFF state currents, which will in turns rise the static power dissipation of the device significantly.

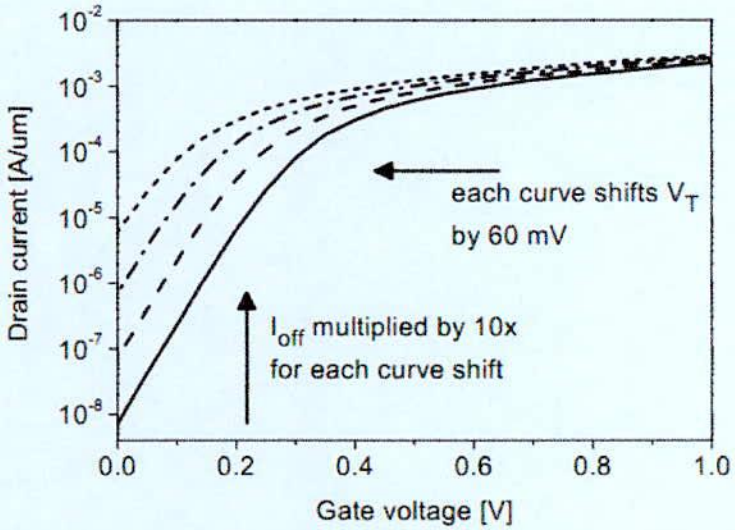

Figure 1.4: A typical I_{DS}-V_{GS} curve for a highly-optimized conventional MOSFET, showing the subthreshold slope limited to 60 mV/decade at room temperature. If we want to decrease V_T by shifting the curve left, we pay a price in leakage current. Solid curve's data [5].

Why the power dissipation is a problem? There are quite a few reasons for which circuits should use less energy, some of which will be mentioned here. The first can be seen on a global scale. We would like our computers, appliances, and gadgets to use less power because it's better for the environment. On a more personal level, it's less expensive to use less electricity. On a practical level, it's more convenient for battery-operated gadgets because their batteries will last longer before needing to be charged. And on a comfort level, it is better when laptops and hand-held gadgets have a lower power density and therefore produce less heat. Looking at Fig.1.5, the trend of increasing power for Intel computer chips is shown. If we assume that chips tend to be on the order of 1 to 2 cm^2, we can get a rough idea of the power density as well. According to [6], published in 2010, current power density is around 60-80W/cm^2. An ITRS presentation predicted that the power density for the 14 nm node would be greater than 100 W/cm^2 [7]. Fig. 1.5 also shows on its right axis that in order to cope with the increasing power density, the heat

sink must grow in volume. This too has a limit, since we would like our appliances, computers, and gadgets to stay the same size or shrink, not get larger in order to accommodate a large heat sink required by the power-hungry chip inside.

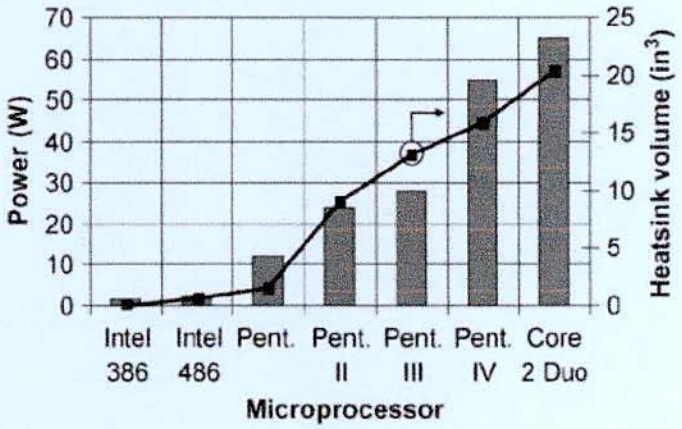

Figure 1.5: Computer chip power trends, along with the accompanying increase in heat sink volume. From [6].

The conclusion of the discussion stated earlier is that we need a device (which may be a MOSFET or something other) having a subthreshold swing less than 60 mV/dec, which depends on the way in which a device produces their current in subthreshold region. For MOSFET we need to understand the Fermi-Dirac distribution function, which describes the probability of the occupation of energy levels by electron which is plotted in Fig.1.6 against E-E_F, where the probability of of energy level occupation is 50% at E-E_F = 0 eV. At absolute zero temperature the, probability of Fermi-Dirac distribution function would be 100% for energy less than the Fermi level and 0% for the energies more than Fermi level, which makes the function perfectly abrupt. As temperature rises the function becomes less abrupt, as can be seen in Fig.1.6

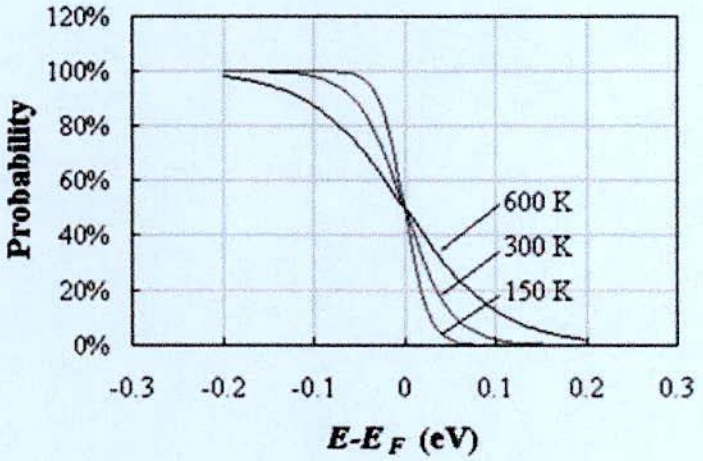

Figure 1.6: The Fermi-Dirac probabilities as a function of energy, for different temperatures, From [8].

The Fermi-Dirac distribution function can be represented mathematically

$$f(E) = \frac{1}{1 + e^{(E - E_F)/\ kT}} \tag{1.1.3}$$

This function determines the rate of increase of carrier in the channel as function of gate voltage, which is limited by kT/q. The Fermi-dirac probability can be seen in the subthreshold current equation of MOSFET [9].

$$I_d \propto e^{\frac{(V_{GS} - V_T)}{m(kT/q)}} \tag{1.1.4}$$

where the kT/q term limits the rate of increase of the current with applied voltage. Solving for subthreshold swing we get

$$S = \frac{dV_g}{d(\log I_d)} = \ln(10)\frac{mkT}{q} \tag{1.1.5}$$

where m is the body effect, whose value is close to 1 for a well-optimized device. Then

$$S = \ln(10) \times 26mV = 60\text{mV/dec} \tag{1.1.6}$$

Since the subthreshold swing is inherently tied to the physical mechanism by which current is generated inside the device in subthreshold, in order to change this limit for swing, it is necessary to change the physical mechanism of the device.

In the the recent years researcher are trying to explore new materials and as well as new mechanism to replace the existing CMOS technology and suppress its drawbacks. Tunneling field effect transistor (TFET), which works on the basis of band to band tunneling are drawing mass attention due to their lower subthreshold swing and low off state leakage current [10] [11] [12] [13] [14] [15] [16]. Since the basis of operation of TFET is band to band tunneling, TFET is more immune to short channel effect than its MOSFET counterpart [17] [18] [19]

1.2 Advent of Tunneling FET

Although the principle of band-to-band tunneling was discovered in 1957 by L. Esaki [20] and the first gated p-i-n structure was proposed in 1978 [21], the interest in the first results on TFETs [22] [23] [24] [25] [26] [27] [28] was limited. This changed rapidly after W. Hansch and I. Eisele et al [29] started to investigate the TFET in 2000. J. Appenzeller et al. found in 2004 [30] that, the TFET might provide a means to overcome the 60 mV/dec switching limit of the classical MOSFET. Following these initial results, several groups started to study the theoretical aspects of TFET operation, which were the impact of the channel dimensionality [31], power consumption [32], phonon scattering [33], temperature dependence [34], gate overlap [35], threshold voltage [36], performance comparison to CMOS [37], heterostructure TFETs [38] [39] [40] [41], strain [42] and general modeling [43]. While Appenzeller's results were obtained with carbon-nanotube FETs, the adoption of the operating principle to silicon FETs seems to be more attractive because the mature silicon technology could offer a straight route to industrial application. Therefore, similar to the early work, most recent experiments focus on silicon and germanium TFETs [44] [45] [46] [47] [48] [49]. Furthermore, C. Hu proposed a slightly

modified TFET structure, which exploits the vertical electric field to create a tunnel junction [50]. The facts how the TFET could overcome the 60mV/dec switching-limit of the MOSFET are discussed in the next chapter.

1.3 Challenges and Scopes in TFET:

In spite of several advantages of TFET's over conventional MOSFET, TFET suffers from a serious problem need to be overcome, which is its low ON state current due to tunneling barrier. Some literature reviews regarding the status of TFET research have been summarized in Table 2.1. Here some of the significant reported results from the year of 2010 to 2015 are presented on TFET. Considering the ON state performance the results from KAUST in 2015 [51] having ON current of 1000 mA/mm with subthreshold slop of 28 mV/dec seems pretty promising. But the problems lies with its technology as mentioned here that is core-shell nanowire, which is very difficult to fabricate on the fabrication point of view. The second highest ON current is reported by Pennsylvania state university in 2012 [52] having ON state current of 135 (mA/mm), though, its subthreshold slope performance is very poor (in the range of 230-350 mV/dec). The technology used here is the vertical transistor technology. For a single transistor, it seems good but when it is required to fabricate a chip then we must move towards the planner technology. And here it is seen, the reported results with planner technology by intel in 2011 [53] does not seems so attractive to drive a chip. Other reported results shown in the table also provides very low ON state current to meet ITRS roadmap for 2024 (ON state current of 3001 mA/mm with subthreshold slope of 40 mV/dec). Beside that the reproducibility of III-IV materials used here in the nanoscale limit is very poor.

Table 1:1Trends and status of TFET research

Year	Affiliation	Technology	Material	I_{ON} (mA/mm)	SS (mV/dec)	Ref.
2015	KAUST	Core-shell NW	InAs/Si	~1000	28	[51]
2013	MIT	Vertical single gate	InGaAs-GaAsSb	0.5	140	[54]
2013	Hokkaido Univ.	Vertical hetero NW	InAs/Si	1	21	[55]
2012	Penn State	Vertical, Single Gate	GaAsSb-InGaAs	135	230-350	[52]
2012	Hokkaido Univ.	Vertical hetero NW	InAs/Si	0.005	21/114	[56]
2012	IBM	GAA NW	InAs/Si	2.4	150	[57]
2011	IBM	GAA NW	InAs/Si	0.4	220	[58]
2011	Notre Dame	Vertical	InGaAs	20	130	[59]
2011	Intel	Planar	InGaAs	~7	60	[53]
2010	Penn State	Non Planar Single Gate	InGaAs	0.4	100-216	[60]

It is therefore very much important to search for proper material system for TFET. Carbon nanotube has a potential to be the appropriate channel material to replace Si or III-V in this new technology due to its unique quasi one dimensional properties such as high electron mobility and high Fermi velocity [32]. Some works has also been done on CNT TFET providing 10^{-7}A tunneling current with 40 mV/dec subthreshold slop at gate bias of 1.5 V [61], 10 μA/μm at gate bias of 0.8 V [62]. Since the tunneling transistor is a new type of device it is of utmost important to explore the performance of this device with different structures and parameters and

search for optimized condition giving the high ON state current to meet the upcoming demand of ITRS roadmap.

1.4 Objectives of this thesis:

The primitive objectives of the research are to model and simulate two double gate CNT TFET structures called OXOC and OXESD structures with the variation of device parameters and isolate their effect on the performance of the proposed TFETs and also search for the optimum value of parameters for highly optimized TFET structures. And then compare between OXOC and OXESD structures in optimized condition to find which one gives the better results. To determine the performances of these devices we used well established open source software Nano_TCAD ViDES. The whole works are carried out as follows:

- The performance of the devices is studied with the variation of the doping density at the source and drain taking into account of uniform doping concentration.
- To determine the optimum oxide thickness and its strength in order to have better performance of the devices.
- The effect of gate underlap in determining the performance of the devices is studied.
- To find out the channel length dependent performance of the devices.

The final objective is to compare the performance of the two devices under optimized condition to realize the best TFET structure on account of transfer characteristics, ON/OFF current ratio and subthreshold swing.

1.5 Thesis Layout

The entire thesis is organized into several chapters where 1 starts with the problems with the existing convention FET technology and their possible solution. The history of TFET technology is discussed and the various challenges of this new type of devices are addressed.

Chapter 2 starts with the importance of numerical simulation to investigate the performance of semiconductor device in Nano scale regime. Then we discussed the operation and some mathematical properties of TFET and discussed the proposed TFET structures. After that, the technique for solving the NEGF and Poisson's equation self-consistently is discussed widely.

In chapter 3, the details results and discussion have been presented. First we observed the behavior of the proposed device under the variation of different parameter and searched for optimized condition. Then we compared the two proposed devices in optimized condition and set a conclusion of better device. In order to do so, we first we calculated their I-V characteristics and then explained their behavior by band diagram and distribution of electric fields and finally compared between two devices.

Finally, in chapter 4, the concluding remarks and recommendation for future work is presented.

Chapter 2 : DEVICE STRUCTURE, PHYSICS AND MATHEMATICAL MODELING

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Chapter Outlines

- **Introduction**
- **Tunnel FET structures and operation**
- **Subthreshold swing of Tunneling FET**
- **BTBT transmission co-efficient**
- **Proposed Double gate CNT TFET CNT TFET structures**
- **A brief premier of NEGF formalism**

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2.1 Introduction:

Numerical device simulation is an important procedure for the design and optimization of novel semiconductor devices. Prior to the device fabrication stage, the numerical simulation of the projected device helps to optimize the design parameters of the device. In simulation a physical system is modeled and then simulated incorporating different system parameters. It can be used to explore and gain new insights into new technology and to estimate the performance of the systems which is too complex for analytical solutions. The advanced miniaturization in the semiconductor technology requires an upgrade of conventional simulation models because several quantum mechanical effects like tunneling through potential barriers or particle accumulation in quantum wells or complex interaction among different parts of the devices appear in these nanometer scaled structures which are difficult to explain by classical theories. It is therefore critical that the research in this area is necessarily be coupled with theoretical perspective in order to resolve these issues, which will help in further enhancing its progress. Running a computer based simulation is also cost effective in comparison with fabrication and performing different types of measurements.

2.2 Tunnel FET structures and operation

In this section the proposed TFET structures and working principle of the TFET are explained based on semi-classical picture. The device structure of the TFET resembles that of the MOSFET with one exception. While in the MOSFET, source and drain are doped with the same type of dopant, in the TFET, source and drain are of opposite doping types. Here we study a n-channel TFET device which has a p-doped source and a n-doped drain and turns on for high gate bias. A typical TFET device structure and I_D-V_{GS} characteristics along with the different states of drain current indicated by a, b and c are shown in Fig.2.1 and Fig.2.2. The energy band diagram corresponding to the indicated regions are also shown in Fig.2.2. Under equilibrium condition the

p-i and n-i junctions result in a staircase-like band profile. In the presence of small drain bias and in the absence of gate bias the electron and hole conductions will be blocked because of the presence of energy barrier between the valance band of the source to the conduction band of the channel shown in Fig.2.1 (a). This is called the OFF state of the device.

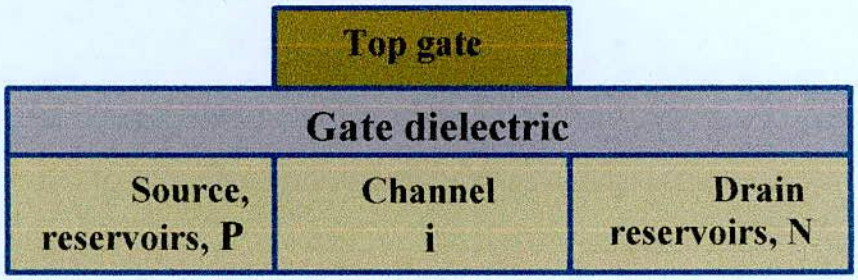

Figure 2.1: A typical Tunnel FET device structure, a p-i-n diode with one gate

As the gate bias is applied gradually, it pushes down the band in the channel region and a position is reached where the C.B of the channel just come to the same level of the V.B of the source. So a condition is reached where electrons can just go from the V.B of the sources to the C.B of the channel. This is called the subthreshold state of the TFET and shown in Fig.2.2(b).

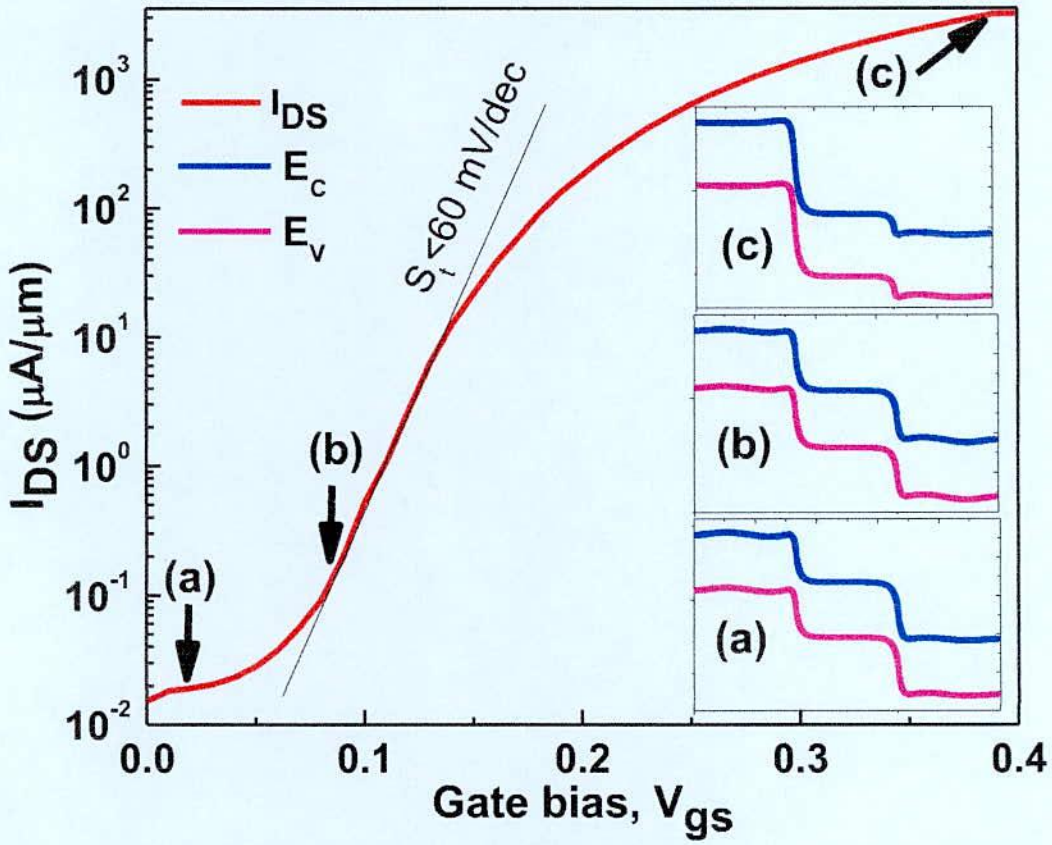

Figure 2.2: A typical I_D-V_{GS} characteristics of simple Tunnel FET with (a) OFF (b) Subthreshold and (c) ON state band diagram.

When sufficiently high voltage is applied in the gate terminal, the energy band in the channel move down further and tunneling occurs at the source-channel junction as soon as the conduction band in the channel is pushed below the valence band of the source. This is the ON state of the device shown in Fig.2.2(c). In this state a significant portion of the V.B of the source is got overlapped with the C.B of the channel. This is the operating principle of n-channel TFET because here electron is accumulated at the channel and we apply the positive bias at both gate and the source terminals. For a p-channel TFET we apply negative voltage.

For larger negative V_{DS} values, saturation occurs similar to the MOSFET case, but for large V_{DS} values in combination with only moderate V_{GS}, it is even possible to create a potential

profile, where tunneling occurs at both junctions simultaneously, resulting in an exponential increase of I_D with V_{DS}. In the device like the TFET, both the n and p-channel operations when found in a single device, is called ambipolar.

To complete this overview of different operation regimes of the TFET, positive V_{DS} bias has to be considered. For sufficiently large positive V_{DS}, the p-i-n -structure is forward biased, which means that without applied gate voltage both electron and hole currents can flow and result in exponential diode characteristics. With gate bias applied, either the electron or the hole current can be blocked by a potential barrier but not both at the same time. Therefore this mode of operation cannot be used for switching, though it might be possible to create a negative differential resistance as observed in Esaki-diodes [63]

2.3 Subthreshold swing of Tunneling FET

The gate voltage dependency of subthreshold slope of tunneling FET is shown in Fig. 2.3. This figure manifests two important facts, which are:

- The value of subthreshold swing for the tunnel FET is not constants and it varies with the gate voltage.
- At lower gate bias it is possible to turn on a tunnel FET with a subthreshold slope lower than the 60 mV/decade limit at room temperature.

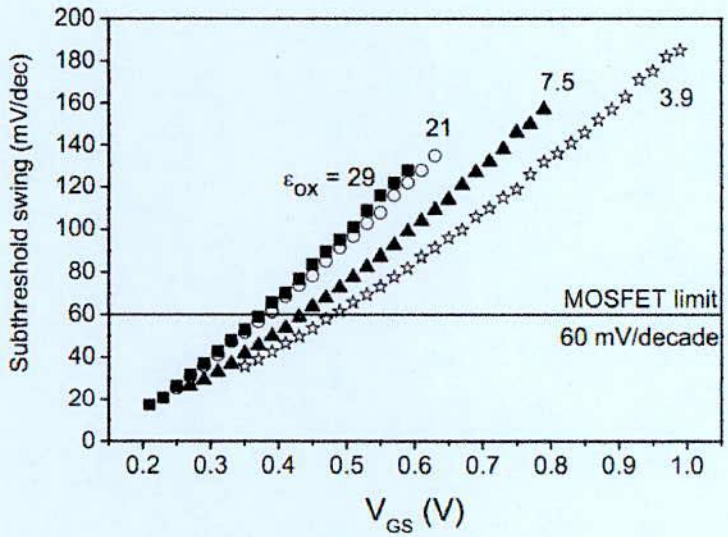

Figure 2.3: Gate voltage dependency of subthreshold slop of tunnel FET for different dielectric constants [2].

The facts stated above can be supported by the following mathematical expression. The tunneling currents equation of reversed biased p-n junction can be given by Sze [64].

$$I = aV_{eff} F \exp(-\frac{b}{F}) \tag{2.3.1}$$

where $a = Aq^3\sqrt{2m^*/E_g}/4\pi^2\hbar^2$ and $b = 4\sqrt{m^*/E_g^{3/2}}/3q\hbar^2$ (2.3.2)

V_{eff} is the bias at the tunnel junction and F is the electric field at the tunnel junction [65]. When the subthreshold slope is calculated as $S = dV_{GS}/d(\log I_{DS})$ we get following expression for subthreshold slop:

$$S = \ln 10[\frac{1}{V_{eff}} \cdot \frac{dV_{eff}}{V_{GS}} + \frac{F+b}{F^2} \cdot \frac{dF}{dV_{GS}}]^{-1} \tag{2.3.3}$$

Several conclusions can be drawn from this equation. First: it should be noted that in sharp contrast with a conventional MOSFET, the subthreshold swing is a function of V_{GS}. This means that the subthreshold region does not appear as a straight line when I_{DS}-V_{GS} is plotted on a

log-lin scale, and the swing does not have one unique value. Swing is smallest at the lowest V_{GS}, and increases as V_{GS} increases.

2.4 BTBT transmission coefficient

The parameter that actually determines the current is the transmission co-efficient. In case of tunnel FET we call it tunneling co-efficient. Using the WKB approximation and taking into account of triangular shaped potential barrier shown in Fig.2.4, the tunneling co-efficient can be deduced.

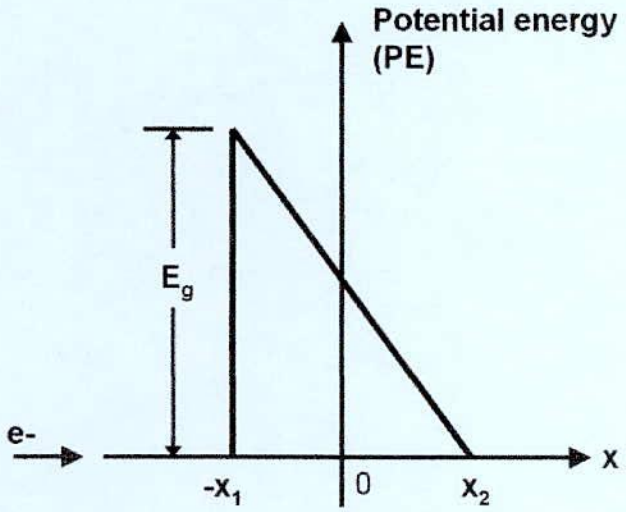

Figure 2.4: BTBT coefficient can be calculated by approximating the energy barrier width by the triangular potential barrier, where electron must tunnel through the widest distance. Redrawn from. Redrawn from [66]

According to WKB approximation, the BTBT transmission co-efficient is given by:

$$T_t \approx \exp[-2\int_{x1}^{x2} |k(x)|\,dx] \qquad (2.4.1)$$

where, $k(x)$ is the quantum wave vector of the electron inside the barrier. Inside the triangular barrier the wave vector is:

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(PE - E)} \tag{2.4.2}$$

Here PE is the potential energy and E is the energy of the incoming electron. When the triangular barrier is drawn at the coordinates shown in "Fig. 2.4", with the electron at the energy of the widest part of the triangle (at $E=0$), then the E term goes away, and PE can be replaced by the equation for the triangle: $E_g/2 - qF_x$ where E_g is the band gap of the semiconductor material at the tunnel junction, and F_x is the electric field. Then,

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(\frac{E_g}{2} - qF_x)} \tag{2.4.3}$$

Plugging this equation into the equation of tunneling co-efficient, we get

$$T_t \approx \exp[-2\int_{x1}^{x2}(\frac{2m^*}{\hbar^2}(\frac{E_g}{2} - qF_x)dx] \tag{2.4.4}$$

After carrying out the calculation we get,

$$T_t \approx \exp[\frac{4}{3}\frac{\sqrt{2m^*}}{q\varepsilon\hbar}(\frac{E_g}{2} - qF_x)^{3/2}]|_{-x_1}^{x_2} \tag{2.4.5}$$

Looking back at the triangular barrier we know that at $x=x_2$, $E_g/2 - qF_x = 0$ and that at $x=-x_1$, $E_g/2 - qF_x = E_g$, So

$$T_t \approx \exp(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\hbar F}) \tag{2.4.6}$$

Where m* is the effective electron mass of the material, E_g is the band gap of the channel material and F is the electric field in the source channel junction. Equation 2.4.6 implies that, the lower electric field will result in lower transmission coefficient and finally lower ON current.

2.5 Proposed double gate CNT TFET structures

2.5.1 **Without gate underlap**

The two double-gate CNT TFET structures investigated in the present study are shown in Figs. 2.5(a) and 2.5(b). The difference between the two structures mainly depends on the construction of the gate dielectric oxide. In one structure we placed the gate oxide only under the gate and we call it CNT TFET with oxide only on the channel or OXEC structure which is shown in Fig. 2.5(a). In another structure gate oxide is extended from source to drain and we call it CNT TFET with oxide extended over source to drain or OXESD structure and shown in Fig. 2.5(b). In the channel of the devices, we have used CNT with chirality (13,0) having a length of 15 nm. CNT in this chirality has a band gap of 0.75 eV and diameter of 1 nm. Source and drain reservoirs are the extensions of the channel with p and n type dopant respectively, having doping density $f_d = 5 \times 10^{-3}$, which means source and drain are doped with 5 dopant atoms among 1000 carbon atoms. As the gate dielectric we used the HfO_2 of the thickness of 2 nm with k=16 whose equivalent oxide thickness (EOT) is 0.5 nm. The simulation is carried out at constant temperature of T=300K. These parameters (doping density, channel length, EOT and temperature) are kept constant for the simulation unless specified otherwise.

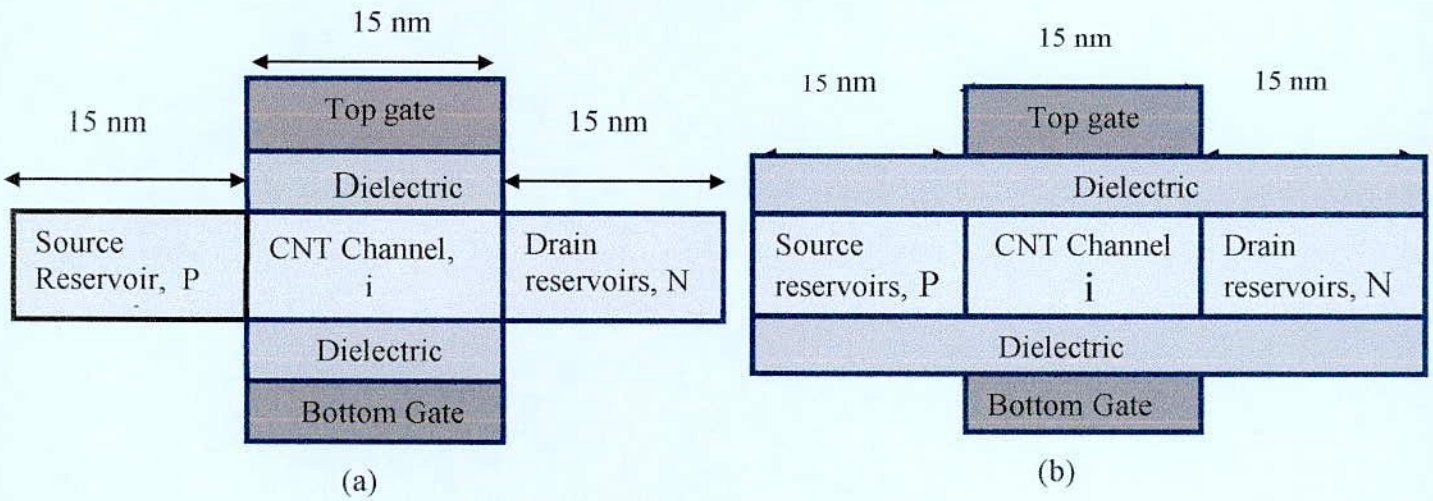

Figure 2.5: Proposed Double gate (a) OXOC and (b) OXESD CNT TFETs structures without gate underlap.

2.5.2 With gate underlap

In Figs. 2.5(a) and (b) we didn't consider the gate underlap that is the portion of the gate uncovered by gate dielectric. In this structure all device parameter are kept same, the only difference is that here a portion of the gate is kept uncovered by the gate. The structures of OXOC and OXESD CNT TFET with gate underlap are shown in Figs. 2.6(a) and (b) where the uncovered portion is denoted by, u_n. Here B.G indicates bottom gate while T.G indicates top gate.

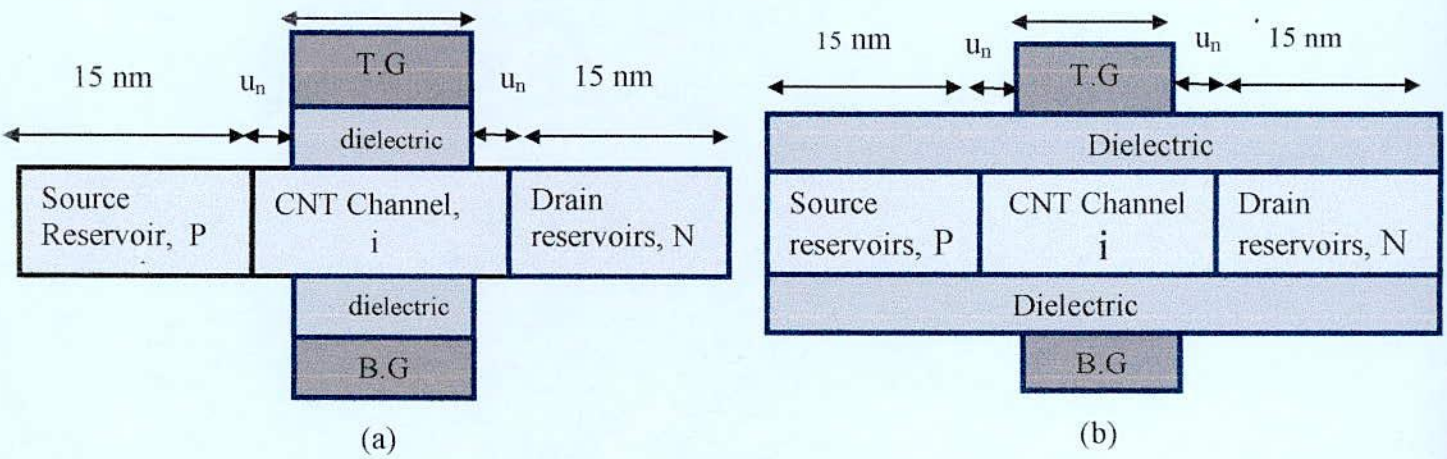

Figure 2.6: Proposed Double gate (a) OXOC and (b) OXESD CNT TFETs structures with gate underlap

2.6 A brief premier of NEGF formalism:

In order to go beyond the WKB model, there are two relevant competing modeling techniques, one is the Monte-Carlo technique [67] [68] and the other one is the direct solution of the Schrödinger and Poisson equations by using the Non-Equilibrium Green's Function (NEGF) [69] [70] approach. Monte-Carlo techniques are most suited for the simulation of long devices where transport is dominated by scattering. The starting point for Monte-Carlo simulations is

usually the Boltzmann-transport equation, which is a classical transport equation and does not include quantum effects. Therefore, tunneling models are introduced phenomenologically and are not necessarily based on first principles. However, Monte-Carlo simulations provide excellent descriptions of all particle interactions, i.e. Coulomb, phonon and photon-scattering.

The NEGF approach on the other hand is fully based on first principles and naturally includes quantum effects like quantization and tunneling. However, due to computing limitations, NEGF is usually limited to devices on the nanometer scale and the consideration of scattering and two and three dimensional device structures is even more challenging in terms of computation time. As band-to-band tunneling is a quantum effect which occurs on the nanoscale, NEGF is more appropriate for the description of the TFET, which is the reason to choose NEGF simulations for the proposed TFET device structures.

2.6.1 **Basic one-dimensional equations:**

The most basic physical equation to describe the electronic structure of matter is the Schrödinger equation. Though it neglects spin and relativistic effects, its time-dependent form can describe the propagation of non-relativistic electrons in vacuum very well. In the solid-state, however, the huge number of atoms and electrons renders any exact numerical solution impossible. To enable numerical simulations, some simplifications and approximations have to be made:

If energy is conserved, i.e. all scattering processes are elastic, the time evolution can be separated and instead of the time-dependent Schrödinger equation, the time-independent Schrödinger equation is solved. The remaining problem is to find the energy eigen-values and -states of the Hamilton operator *H*.

The periodicity of the crystal lattice is used to reduce the spatial dimension of the lattice to one primitive cell. The corresponding solution of the Schrödinger equation is called 'Bloch

wave'. This assumption implies the conservation of the wave-vector k, which also implies that the scattering conserves the crystal momentum.

Electron-electron interactions are neglected, but a self-consistent field approximation is used instead. The self-consistent potential describes the average potential that one electron experiences due to the presence of all other electrons (Hartree-potential without exchange term). This simplification for example precludes the simulation of Coulomb-blockade.

When using single atom wave functions, the first three assumptions allow for the calculation of the band-structure of crystals. Though band structure calculations are a very active and important field of research, including the full band structure in transport simulations is computationally very intensive and goes beyond the scope of this work. To simplify the band structure only one conduction band and one valance band has been included in the simulation. The shape of the bands in k-space is approximated by the effective mass approximation, which is a second order polynomial fit to the real band structure. By using the effective mass approximation, the Schrodinger equation adopts the form of free particle equation. The only difference being that instead of free electron mass, the effective mass is used. As another consequence of the effective mass approximation, independent of the real band structure, all semiconductors are modeled with direct band gap. It means that the phonon assisted nature of the BTBT in indirect semiconductor (Si, Ge, ..) is neglected. However for the room temperature simulations, we can assume that the phonon density is very large and does not limit the tunneling rate. According to [33], even the opposite is the case because phonon can exchange energy with electron and therefore allow for tunneling that is forbidden in ballistic transport, thereby increasing the device current.

The resulting one-dimensional Schrödinger equation is

$$-\frac{\hbar}{2m^*}\cdot\frac{d^2}{dx^2}\psi_E + U(x)\psi_E = E\psi_E \tag{2.6.1}$$

The first term, which comprises the kinetic energy of the wave-function ψ_E with eigen energy E, only depends on the Planck constant and the effective mass. The second term represents the potential energy, here in the form of the self-consistent potential $U(x)$. To determine the self-consistent potential, the second basic equation, the Poisson-equation needs to be solved

$$\frac{d}{dx}(\varepsilon_r(x)\frac{d}{dx}U(x)) = -\frac{\rho(x)}{\varepsilon_0} \tag{2.6.2}$$

This equation states the proportionality of the second derivative of the self-consistent potential to the electric charge density $\rho(x)$ divided by the dielectric constant of vacuum ε_o. For later use, the relative dielectric constant $\varepsilon_r(x)$ is assumed to vary spatially.

2.6.2 **Length scale potential variation:**

In order to describe a two-dimensional transistor channel correctly, in principle a two-dimensional Poisson equation is solved. While this method has to be employed for bulk-transistors, for devices with a limited vertical extent like thin body silicon-on-insulator or nanowire structures an even simpler approach can be used. Under the assumption that the vertical potential varies much slower than the lateral potential, the vertical potential can be approximated by a second order polynomial, with the only parameter being Λ, the effective screening length for lateral potential variations [71]. The result is an effective one-dimensional Poisson equation, that incorporates the effect of the gate:

$$\frac{d^2U}{dx^2} - \frac{U - V_{GS} + V_{bi}}{\Lambda^2} = -\frac{\rho}{\varepsilon_r\varepsilon_0} \tag{2.6.3}$$

Here, V_{GS} is again the gate voltage and V_{bi} is the built-in potential which is due to the work-function difference in the MOSCAP structure. From this differential equation, the

importance of Λ for the TFET becomes apparent, since Λ determines the steepness of the potential profile. Λ is calculated differently for different device geometries. For a thin body SOI device, Λ is:

$$\Lambda_{SOI} = \sqrt{d_{Semi} d_{Insu} \varepsilon_{Semi} / \varepsilon_{Insu}} \tag{2.6.4}$$

For a coaxial gate-all-around nanowire, however, Λ is smaller:

$$\Lambda_{NW} = \sqrt{\varepsilon_{Semi} / 8\varepsilon_{Insu} \, d_{semi}^2 \ln(1 + 2 d_{Insu} / d_{Semi})} \tag{2.6.5}$$

In both expressions, ε_{Semi} and ε_{Insu} represent the relative dielectric constants of the semiconductor and the gate insulator, respectively. d_{Semi} and d_{Insu} are the thicknesses of the SOI or nanowire and the gate insulator.

2.6.3 **Finite difference method**

SCHRODINGER equation:

The two basic differential equations needed for transport simulations are described in equation (2.6.1) and (2.6.2). The numerical method for solving these equations is presented here. The first step for a numerical solution of the Schrödinger and Poisson equation is to define a spatial lattice on which the wave-function and the self-consistent potential can be defined by,

$$\{\psi\} = \begin{pmatrix} \psi \\ . \\ . \\ \psi_N \end{pmatrix} = \begin{pmatrix} \psi(x_1) \\ . \\ . \\ \psi(x_N) \end{pmatrix} \tag{2.6.6}$$

Here $\{\psi\}$ is a vector that represents the wave-function ψ evaluated at the sites of a one dimensional lattice $x_1 \ldots . x_N$ with spacing a. The self-consistent potential U is expanded in the same way but for simplicity it is set to a constant value U_o in the following discussion. In this

expansion, the Hamilton operator is represented by a matrix *[H]* which in its simplest form only regards nearest neighbor couplings:

$$[H]\{\psi\} = E\{\psi\} \tag{2.6.7}$$

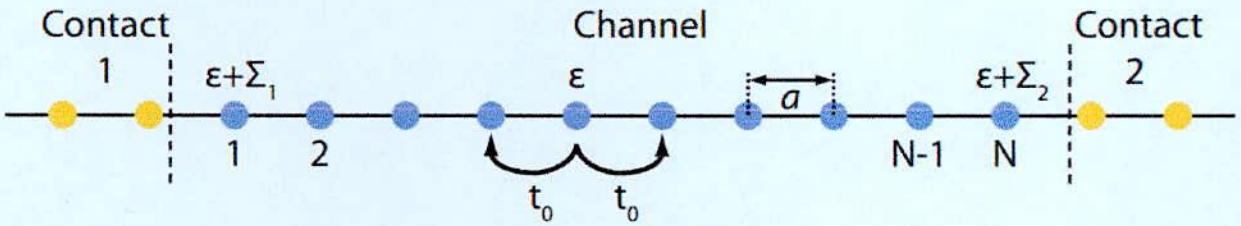

Figure 2.7: One dimensional NEGF simulation domain. All lattice sites with spacing a is connected to each other by the nearest neighbor coupling to. the semi-infinite contact is considered by a self-energy term, Σ that adds the first and last site of the simulation domain.

With

$$[H] = \begin{pmatrix} \varepsilon & -t_0 & & & \\ -t_0 & \varepsilon & \ddots & & \\ & \ddots & \ddots & -t_0 & \\ & & -t_0 & \varepsilon & -t_0 \\ & & & -t_0 & \varepsilon \end{pmatrix} \tag{2.6.8}$$

By comparison with the differential form of the stationary Schrödinger equation, the on-site energy ε and the nearest neighbor coupling strength t can be evaluated to

$$t_0 = \frac{\hbar^2}{2m^* a^2} \text{ and } \varepsilon = 2t_0 + U_0 \tag{2.6.9}$$

For a single lattice site, the matrix equation corresponds to

$$E\psi_n = -t_0\psi_{n-1} + \varepsilon\psi_n - t_0\psi_{n+1} \tag{2.6.10}$$

In this form, it becomes obvious that only nearest neighbors with the indices *n-1* and *n+1* are considered in the numerical solution, which is therefore also called a 'tight-binding' approach. To derive an *E-k* relation for the matrix representation of the Schrödinger equation, a plane-wave ansatz for ψ_n is used.

$$\psi_n = e^{ikx_n} = e^{ikna} \tag{2.6.11}$$

The resulting E-k relation is:

$$E = \varepsilon + 2t_0 \cos(ka) \tag{2.6.12}$$

This solution represents a cosine-shaped band, which for small *ka* resembles the parabolic E-k relation of the free-electron Schrödinger equation

$$E = \varepsilon + 2t_0 - t_0^2 a^2 k^2 = \frac{\hbar^2 k^2}{2m^*} + U_0 \tag{2.6.13}$$

While in vacuum the parabolic *E-k* relation is exact, in the solid-state the cosine-shaped band of "equation (2.6.12)" is a more accurate description, because it takes into account the finite width of the bands as well as the different curvatures at the top and the bottom of the band.

Poisson equation:

Following the example of the Schrödinger equation, the Poisson equation, which is also a second order differential equation, can be turned into a matrix equation in a similar fashion. Here for constant ε_r the equation can be expressed by

$$\frac{1}{a^2}[U(x_{i-1}) - 2U(x_i) + U(x_{i+1})] = -\frac{\rho(x_i)}{\varepsilon_r \varepsilon_0} \tag{2.6.14}$$

This matrix representation makes the numerical solution of these equations very simple and automatic. For any arbitrarily shaped potential, the only challenge is to write down the corresponding matrix. The actual solution is reduced to an Eigen-value problem which can be computed easily.

2.6.4 **Boundary condition- $S_{CHRODINGER}$ equation**

So far, the finite-difference scheme that has been described suffers from one limitation. It is restricted to a lattice of finite dimension, which means that the simulation domain is encompassed by impenetrable regions that the wave-function cannot enter. While this behavior is appropriate for most problems involving a potential well, for transport in semiconductors it is unacceptable. Instead the concept of semi-infinite leads, which assumes that the simulation domain ('channel') continues infinitely on one or both ends, is very useful. To include semi-infinite domains, without at the same time increasing the dimension of the corresponding matrices to infinity, the self-energy method has been developed (see "Fig. 2.7").

To illustrate the concept of 'self-energy' Σ, we assume a channel with only one lattice point $n = 0$ and a semi-infinite contact that is attached on the left site: $n = -1 \ldots -\infty$:

$$E\psi_0 = \varepsilon\psi_0 - t_0\psi_{-1} \tag{2.6.15}$$

The semi-infinite contact itself fulfills equation (2.6.10) and with an ansatz that is similar to equation (2.6.11), ψ_{-1} can be expressed as:

$$\psi_{-1} = e^{ika}\psi_0 + B(e^{-ika} - e^{+ika}) \tag{2.6.16}$$

While the origin of the first term can be understood immediately from equation (2.6.11), the second term is a result of a possible reflection at the contact/channel interface. Only a fraction B of the incident wave is transmitted into the channel. Substituting this expression into (2.6.15) shows that the effect of the contact can be included in the onsite energy ('self-energy') of the channel lattice site and a source term S that describes the excitation of the channel by an incident wave from the contact:

$$E\psi_0 = (H + \sum)\psi_0 + S \text{ with } \sum = -t_0 e^{ika} \text{ and } S = it_0 2B\sin(ka) \tag{2.6.17}$$

The main consequence of adding the 'self-energy' term to the Hamilton operator is an open boundary condition. Therefore, any wave-package acquires a finite lifetime, i.e. it can

escape the simulation domain and if it escapes, it never returns. In the energy domain, the finite lifetime causes a broadening of formerly discrete energy-levels. The broadening of the levels, or the inverse life-time of a state, is given by the broadening function:

$$\Gamma(E) = i[\sum(E) - \sum^{+}(E)] \tag{2.6.18}$$

2.6.5 **Boudary conditions- P_{OISSON} equation**

While for the Schrödinger equation open boundary conditions are favorable, the solution of the poisson equation should fulfill a zero field condition, i.e. the first derivative of the self-consistent Potential should vanish (Neumann condition). This condition is necessary to maintain a smooth continuation of the potential into the contacts, which at the same time ensures that no charge builds up at the boundary. Mathematically, the zero field condition is expressed as follows:

$$U(x_{-1}) - U(x_0) = U(x_{N+1}) - U(x_N) = 0 \tag{2.6.19}$$

2.6.6 **Local Density of States**

One of the central properties that the solution of the Schrödinger equation should yield is the charge density. In analogy to the classical calculation of the charge density, we first calculate the Local Density of States (LDOS) and in a second step 'fill' these states according to an equilibrium Fermi-distribution. The LDOS weights each eigen-state by the square of its wave-function at a location r

$$D(r, E) = \sum_a |\psi_a(r)|^2 \delta(E - \varepsilon_a) \tag{2.6.20}$$

This quantity can be identified with the diagonal elements of the spectral function $A(E)$.

$$A(r, r', E) = 2\pi \sum_a \psi_a(r) \delta(E - \varepsilon_a) \psi_a^*(r') \tag{2.6.21}$$

The off-diagonal elements of $A(E)$ can be interpreted as transition probabilities between two positions r and r' at a given energy E. This interpretation is the starting point to calculate

device current from transmission, which is essentially given by the off-diagonal elements of *A(E)*. To evaluate the spectral function, it is convenient to make use of the (retarded) Green's function:

$$G(E)=[(E+i\eta)I-H]^{-1} \tag{2.6.22}$$

In this definition, I is the identity matrix and η is an infinitesimally small quantity that ensures causality. The Green's function acts as an 'inverse' of the Hamilton operator. For example, inhomogeneous solutions of the Schrödinger equation can be calculated from the Green's function and the source term. Using the Green's function, the spectral function becomes:

$$A(E)=i[G(E)-G^{+}(E)] \tag{2.6.23}$$

Indeed if our interest was limited to closed systems there would be little reason to use Green's functions. But for open systems the Green's function method allows us to focus on the device of interest and replace the effect of all external contacts and baths with self-energy functions $\sum_{1,2,S}$ (see "Fig. 2.8") which are matrices of the same size as the device Hamiltonian, even though the contacts themselves are much larger entities. This is one of the seminal concepts of many-body physics that we will now discuss

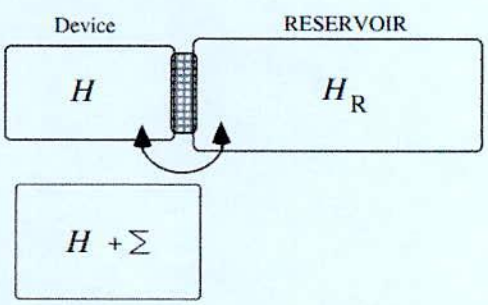

Figure 2.8: The interaction of the device with a reservoir can be represented by a selfenergy matrix Σ. Taken from [72]

The open boundary conditions are handled in the self-energy matrices Σ_S and Σ_D, where the indexes s and d denote for source and drain respectively. With the nearest tight-binding model, the nonzero values in the Σ_s and Σ_d matrices are $(n \times n)$. The self-energy represents the coupling between the device and the contacts due to the wave function interchange between the device and the outside electronic terminals. The electronic terminals, i.e., the source and drain, are supposed to be semi-infinite long reservoirs in thermal equilibrium characterized with the Fermi levels E_{Fs} and E_{Fd}. The self-energies can be obtained with a recursive relation [73] for the surface Green's function. Note that the self-energies are energy dependent.

The retarded Green's function G is the key quantities in NEGF, and it can be expressed as follows, taking into account the self-energies [74]

$$G = [(E + i0^+)I - H - \sum_S - \sum_D]^{-1} \tag{2.6.24}$$

Here H is the Hamiltonian matrix of the device in an appropriate form. In the CNT device simulation, the nearest p_z orbitals nearest tight binding is adequate, as only the energy of the p_z orbitals is around the Fermi level and relevant in carrier transport. For a $(n,0)$ semiconducting zigzag CNT with N_c carbon rings, the matrix size of H is $(nN_c \times nN_c)$.

As the matrix inversion is needed, the complexity of direct inverting is $O(n^3 \times N_c^3)$ [75]. Obviously, G is also energy dependent and runs on all interested energies. Thus, the calculation of G is very demanding, especially when the matrix size is large. Many efficient techniques have been developed to reduce the computation burden. In the mode-space method [75] [76], the matrices H, Σ and G are all transformed to a mode space. Considering only the lowest N_m ($N_m \ll n$) modes considered, the matrices size will be reduced from $(nN_c \times nN_c)$ to $(N_m N_c \times N_m N_c)$ [76]. In the recursive Green's function (RGF) algorithm, the block tri-diagonal structure is exploited to reduce the complexity from $O(n^3 \times N_c^3)$ to $O(n^3 \times N_c)$ [77]. However, if the gate

leakage current is accounted, the matrices would not be strictly block tri-diagonal. Thus, the high-order elements will be neglected in RGF method underestimating the coupling effect through the gate terminal [78]. The contact block reduction method [79] is another efficient Green's function technique, which reduces the complexity to $(O(N_{eigen} \times N_A^2) + O(N_A^3))$, where N_A is the size of the boundary region coupling with outside contacts ($N_A = 2n$, here considering the source and drain) and $N_{eigen} (N_{eigen} \ll nN_c)$ is the number of eigenstates used in spectral expansion for G.

Once G is obtained, all interested physical entities (e.g., the electron density, n, and the source-to-drain current, I) can be calculated. The electron density n can be calculated as:

$$n = \frac{1}{\pi} \int dE[A_S f(E - E_{Fs}) + A_d f(E - E_{Fd})] \tag{2.6.25}$$

where A_s and A_d are the spectral functions for source and drain, respectively, and f is the Fermi distribution function. The spectral function can be expressed as

$$\begin{aligned} A_S &= G\Gamma_S G^+, \Gamma_S = i(\sum_S - \sum_S^+) \\ A_d &= G\Gamma_d G^+, \Gamma_d = i(\sum_d - \sum_d^+) \end{aligned} \tag{2.6.26}$$

where Γ_s and Γ_d are the broadening matrices for the source and drain. The source-to-drain current can be calculated as

$$I = \frac{q}{\pi\hbar} \int dE T(E)[f(E - E_{F_s}) - f(E - E_{F_d})] \tag{2.6.27}$$

Where $\hbar$ is the reduced Planck's constant and T is the source-to-drain transmission coefficient which is computed as

$$T = Trace(\Gamma_S G \Gamma_d G^+) \tag{2.6.28}$$

Note that the matrices G, Σ, Γ, A, and T are all energy-dependent and needs to be calculated at all relevant energy levels E. The spectral matrix A in equation (2.3.26) and the

transmission coefficient T in equation (2.3.27) are small at very low energy, and the Fermi distribution function f is small for very high energy. Thus, only the intermediate energy levels are relevant in the calculations.

2.6.7 **Self-consistent calculation**

At this point, all essential building blocks of NEGF calculations have been described, therefore this section focuses on how to combine these blocks into a self-consistent calculation.

The Green's function is computed by means of the Recursive Green's Function (RGF) technique [80] [81]. Particular attention must be put in the definition of each self-energy matrix, which can be interpreted as a boundary condition of the Schrodinger equation. In particular, in our simulation we have considered a self-energy for semi-infinite leads as boundary conditions, which enables to consider the CNT as connected to infinitely long CNTs at its ends.

From a numerical point of view, the code is based on the Newton-Raphson (NR) method with a predictor/corrector scheme [82]. In "Fig. 2.9" we sketched a flow-chart of the whole code. In particular, the Schrodinger/NEGF equations are solved at the beginning of each NR cycle, starting from an initial potential $\tilde{\varphi}$ and the charge density in the CNT is kept constant until the NR cycle converges (i.e. the correction on the potential is smaller than a predetermined value). The algorithm is then repeated cyclically until the norm of the difference between the potential computed at the end of two subsequent NR cycles is smaller than a predetermined value.

Some convergence problems however may be encountered using this iterative scheme. Indeed, since the electron density is independent of the potential within a NR cycle, the Jacobian is null for points of the domain including carbon atoms region, losing control over the correction of the potential. We have used a suitable expression for the charge predictor, in order to give an approximate expression for the Jacobian at each step of the NR cycle. To this purpose, we have

used an exponential function for the predictor. In particular, if n is the electron density as in equatiom (2.6.29), the electron density n at the *i-th* step of the NR cycle can be expressed as:

$$n_i = n \exp(\frac{\phi_i - \tilde{\phi}}{V_T}) \tag{2.6.29}$$

where $\tilde{\varphi}$ and ϕ_i are the electrostatic potential computed at the first and *i-th* step of the NR cycle, respectively, and V_T is the thermal voltage. Same considerations follow for the hole-concentration. Since the electron density n is extremely sensitive to small changes of the electrostatic potential between two NR cycles, the exponential function acts in the overall procedure as a dumping factor for charge variations. In this way, convergence has been improved in the sub-threshold regime and in the strong inversion regime. Convergence is still difficult in regions of the device where the charge is not compensated by fixed charge, where the right-hand term of the Poisson equation is considerably large.

An under-relaxation of the potential and of the charge can also be performed in order to help convergence. In particular, three different under-relaxations can be performed inside ViDES:

(i) relaxation on the potential at each NR cycle φ_i

$$\phi_i^{new} = \phi_i^{new} + \varepsilon(\phi_i^{old} - \phi_i^{new}) \tag{2.6.30}$$

(ii) relaxation on the potential at the end of each NR cycle Φ_f

$$\phi_f = \phi_f + \varepsilon(\tilde{\phi} - \phi_f) \tag{2.6.31}$$

(iii)relaxation of the charge density ρ_{NEGF} computed by the NEGF modules

$$\rho_{NEGF}^{new} = \rho_{NEGF}^{new} + \varepsilon(\rho_{NEGF}^{old} - \rho_{NEGF}^{new}) \tag{2.6.32}$$

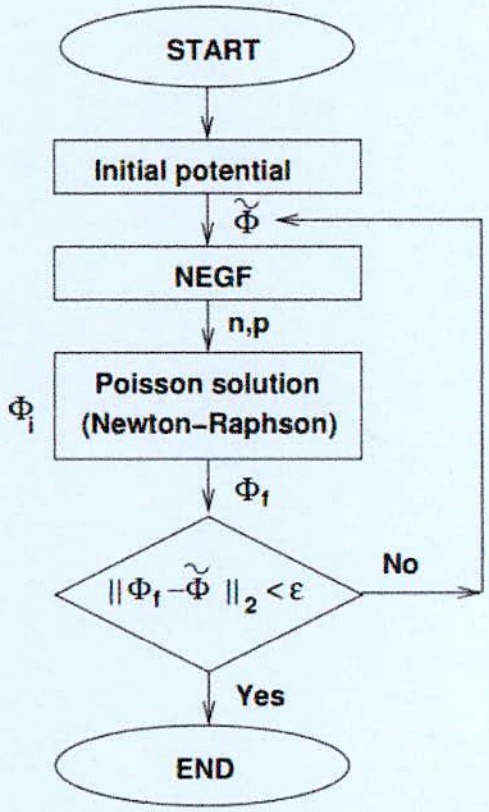

Figure 2.9: Flow-chart of the self-consistent 3D poison-Schrodinger solver

Chapter 3 SIMULATION RESULTS AND DISCUSSION

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Chapter outlines

- **Introduction**
- **Performance of CNT based OXOC and OXESD TFET structure**
    - Gate oxide dielectric strength dependent performance
    - Gate oxide thickness dependent performance
    - Channel length dependent performance
    - Effect of gate underlap
    - Doping density dependent performance
    - Performance comparison between OXOC and OXESD structures in optimized condition.

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3.1 Introduction

This chapter contains the details simulation results of OXOC and OXESD double gate CNT TFET structures. It is to be noted here that the conventional scaling rule of MOSFET (which is constant electric field) is not blindly followed to scale down the tunnel FET. In a previous study Bhuwalka, et al. have explained about the rule of scaling down of the Si TFET and concluded that constant field scaling rule is not applicable for TFET [83], though they have many works where the channel length and oxide thickness are decreased simultaneously [84] [83], following the Dennard's scaling rule. As it is already mentioned that in Dennard's scaling rule requires all the device parameters are to be scaled down simultaneously to keep the electric field inside the device constant. However, when studying TFET, it is more convenient to vary one parameter at a time, in order to get complete understanding of the effect of each change and isolate the effects.

In our study the performances of the devices are studied as a function of gate oxide dielectric strength, its thickness, channel length, gate underlap length and doping concentration. The current voltage (I-V) characteristics are obtained by solving the NEGF and Poisson's equation self-consistently in NanoTCAD_ViDES environment. Other figure of merits such as I_{ON}/I_{OFF} ratio and subthreshold slope are studied from the transfer characteristics. The results obtained from the simulation are explained by energy band diagram along the transport direction and as well as the distribution of electric field at the tunneling junction.

3.2 Effect of gate dielectric constants

In this section the gate dielectric oxide strength dependent performances of the proposed OXOC and OXESD double gate CNT TFET structures are presented. Here the gate oxide thickness is kept constant at 2.0 nm, while the dielectric constants of the gate oxide are varied

from 3.9 to 25. Generally, it is found that gate dielectric oxide with higher dielectric constant improves the performance (ON state current) of a transistor. However in our studies we get an exceptional result, that is the gate oxide material with higher dielectric strength reduces the ON state current of the transistor. Dielectric materials used in our study are listed in "Table. 3.1" along with their dielectric constants.

Table 3.1: Lists of dielectric materials with their dielectric strengths

Dielectric Material	**Dielectric Strength**
Silicon Dioxide (SiO_2)	3.9
Silicon nitride (Si_3N_4)	7.0
Hafnium Silicate ($HfSiO_4$)	11
Yttrium Oxide (Y_2O_3)	16
Hafmium Oxide (HfO_2)	25

To compare gate dielectric oxide strength dependent performance between the two CNT TFET structures, we first present the oxide dielectric strength dependent transfer characteristics of OXOC structure as seen in Fig.3.1, where dielectric constants of the gate oxide are varied from 3.9 to 25. The channel length and the doping density are kept constant at 15 nm and 5×10^{-3}. The curve is plotted in both logarithmic and linear scale to understand the difference between I_{ON} and I_{OFF} clearly.

From Fig.3.1, it is seen that, in OXOC structure, the ON current is the lowest for the smallest dielectric constant and it gradually increases with increase in dielectric strength. This result can be explained from the respective ON state band diagram and distribution of electric fields shown in Fig.3.2 and Fig.3.3, respectively. The ON state band diagram is shown in Fig.3.2 (a). To understand the band to band tunneling distance, the extended view of band diagram corresponding to solid square box is shown in the inset of Fig.3.2 (a). It is seen that the gate

oxide with the lowest dielectric constant offers the longest tunneling distance, W (smallest distance of the same energy level between the valance band of the source and the conduction band of the channel). As a result the tunneling probability becomes minimum, hence the lowest current is obtained. As the dielectric constant increases the barrier width is found to decrease in Fig.3.2. It is clearly observed in Fig. 3.2(b) that the barrier width decreases from 1.26 nm to 0.49 nm for the variation of dielectric strength from 3.9 to 25. This demonstrates that why the ON current increases with increasing dielectric strength of the oxide material.

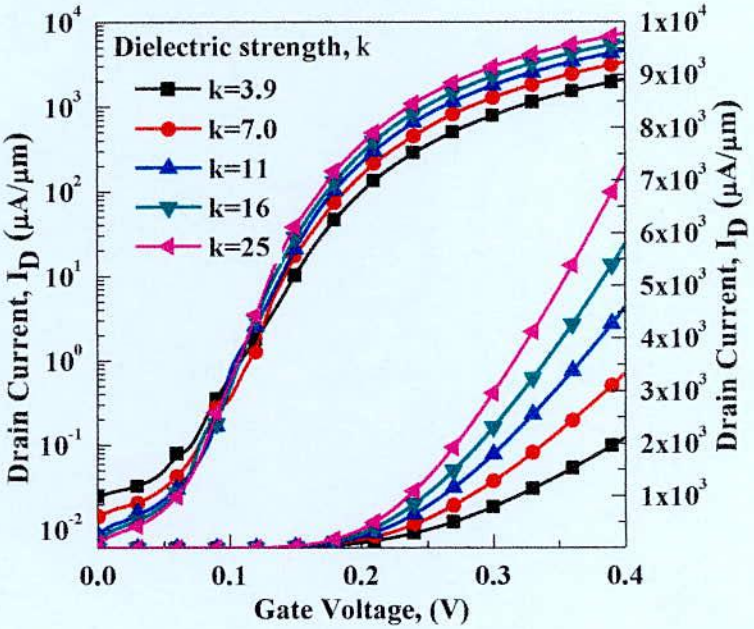

Figure 3.1: I_D-Vgs characteristics of the OXOC structure as a function of different gate oxides having thickness of 2 nm.

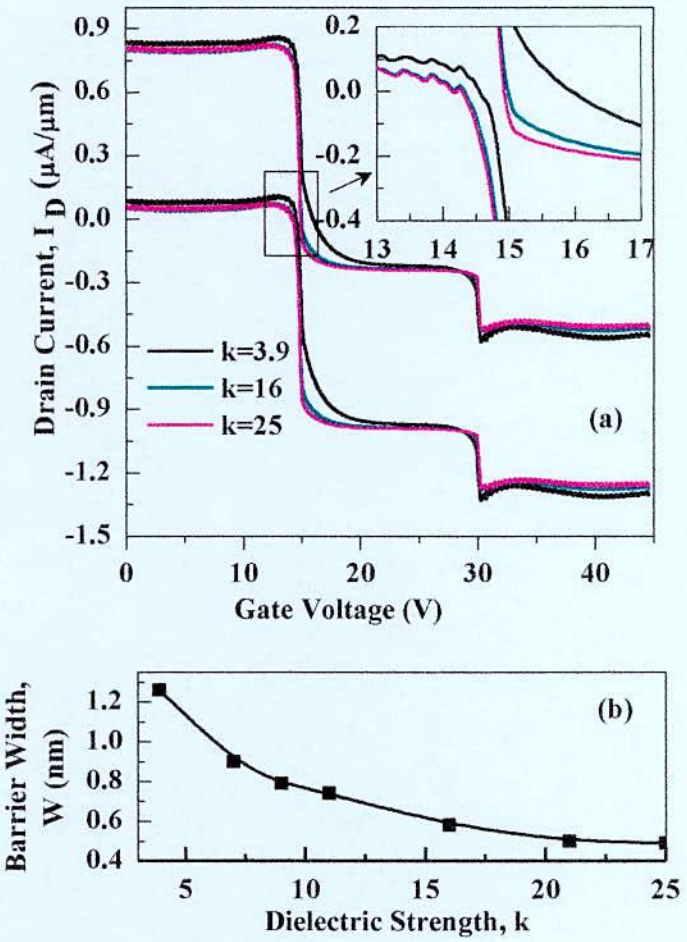

Figure 3.2: (a) ON state band diagram and (b) barrier width as a function of dielectric constants. The results are shown for OXOC structure with oxide thickness of 2 nm

This rising trends of I_{ON} can also be explained from the distribution of electric field at the tunneling junction shown in Fig.3.3. It is found that the peak amplitude of the electric field at the tunneling junction is increased with increasing the value of oxide dielectric constant. According to "Eq.2.4.6" the transmission coefficient also increases gradually with increasing of peak electric field in the tunneling junction for higher dielectric constant, which justifies why the ON state current increases with increasing dielectric constant.

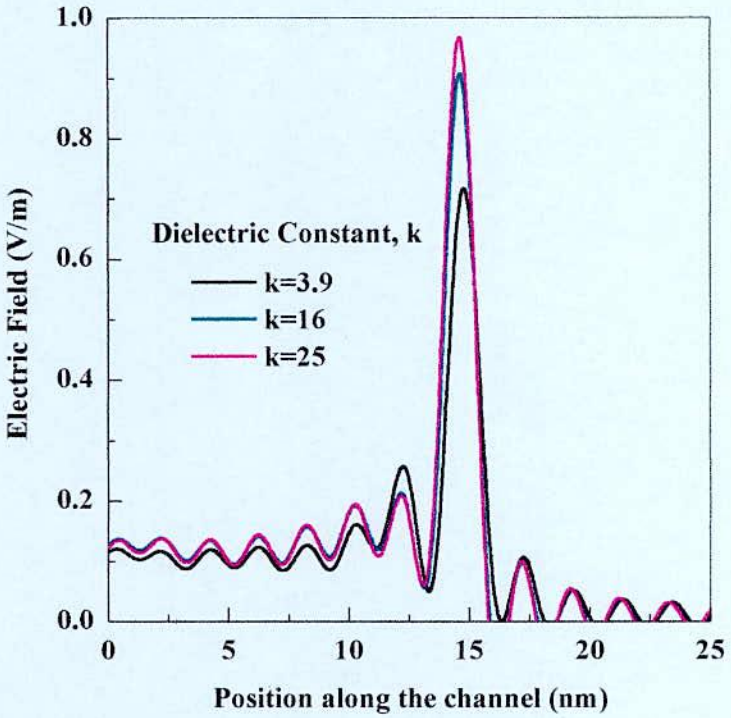

Figure 3.3: ON state electric field distribution for OXOC structure as a function of dielectric constants for k=3.9, k=16 and k=25.

Similarly in the OFF state behavior of the OXOC structure, we see that I_{OFF} have falling characteristics with increasing the value of dielectric constant and it can be explained from the OFF state band diagram shown in Fig.3.4, where the square marked region is shown in the inset. It is seen that the tunneling distance increases gradually with increasing the value of dielectric constant. As a result, the OFF state current is also reduced gradually for the increasing value of dielectric constants for the OXOC structure.

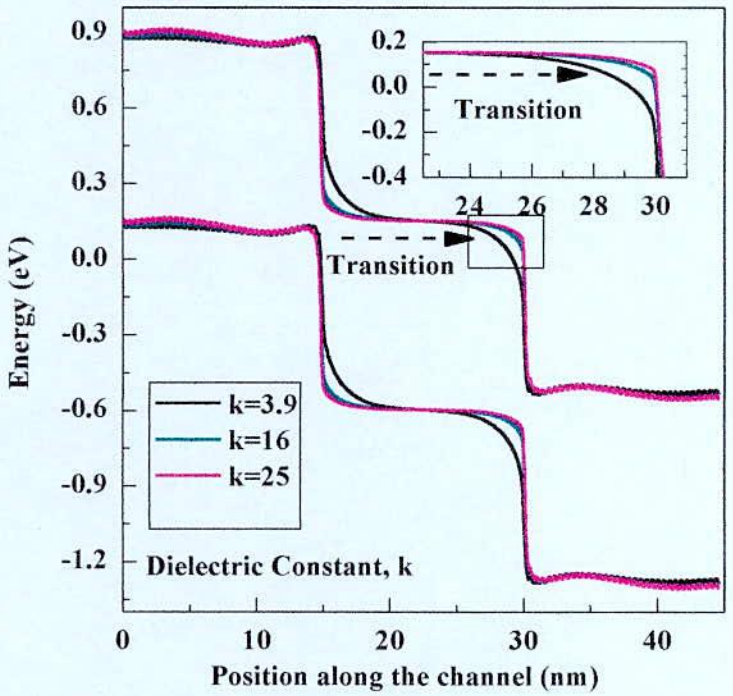

Figure 3.4: OFF state band diagram for different dielectric constants of OXOC structure calculated for the oxide thickness of 2 nm.

In contrast, the gate oxide dielectric constants dependent transfer characteristics of OXESD structure is somehow different from OXOC structure and it is shown in Fig.3.5. Here all the conditions (oxide thickness, gate voltage, drain voltage) are kept same as OXOC structure for fair comparison between them. It is seen that the ON current is the highest for the smallest dielectric constant and gradually decreases with increasing dielectric constants, which is the reverse trends of OXOC structure as discussed before. This result can also be explained from the respective ON state band diagram and distribution of electric field shown in Fig.3.6 and Fig.3.7. From the extended view of the ON state band diagram shown in the inset of Fig.3.6 (a), it is clear that the lowest gate oxide dielectric constant offers the lowest tunneling distance, which in terns results in the highest drain current. As the dielectric constant is increased the barrier width is observed to be increased in OXESD structure shown in Fig.3.6 (a). As a result tunneling

probability reduces, which in turns results in gradual fall of ON state current with increasing the value of oxide dielectric constant. This rising trend of the barrier width is shown pictorially in Fig.3.6 (b).

The distribution of electric field at the tunneling junction shown in Fig.3.7 also supports our results. Here the peak amplitude of electric field at the tunneling junction is observed to be reduced with increase in oxide dielectric strength. This in turns reduces the transmission co-efficient according to "Eqn.(2.4.6)" and hence the reduction of I_{ON} occurs.

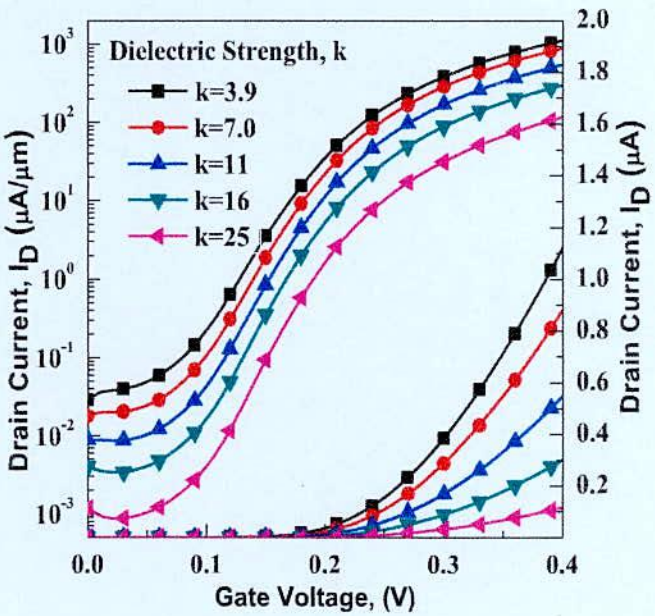

Figure 3.5: I_D-Vgs characteristics of OXESD structure as a function different gate oxide materials having thickness of 2 nm.

Similar to OXOC, OXESD structure shows the falling characteristics of I_{OFF} with increase in dielectric constants and it can also be explained from the respective OFF state band diagram shown in Fig.3.8. Here it is seen that the tunneling distance increases gradually with increase in dielectric constants. As a result, the OFF state current is reduced gradually.

To reveal the dielectric strength dependent trends of ON and OFF currents, I_{ON}/I_{OFF} ratio and subthreshold slope and hence to make a comparison among them for OXOC and OXESD structures, Fig.3.9 is plotted. It is found that the I_{ON}/I_{OFF} has rising trends for both OXOC and OXESD structure with the oxide dielectric constants shown in Fig.3.9(c). For OXOC structure it is quite obvious because here I_{ON} increases while I_{OFF} decreases gradually with increasing dielectric strength.

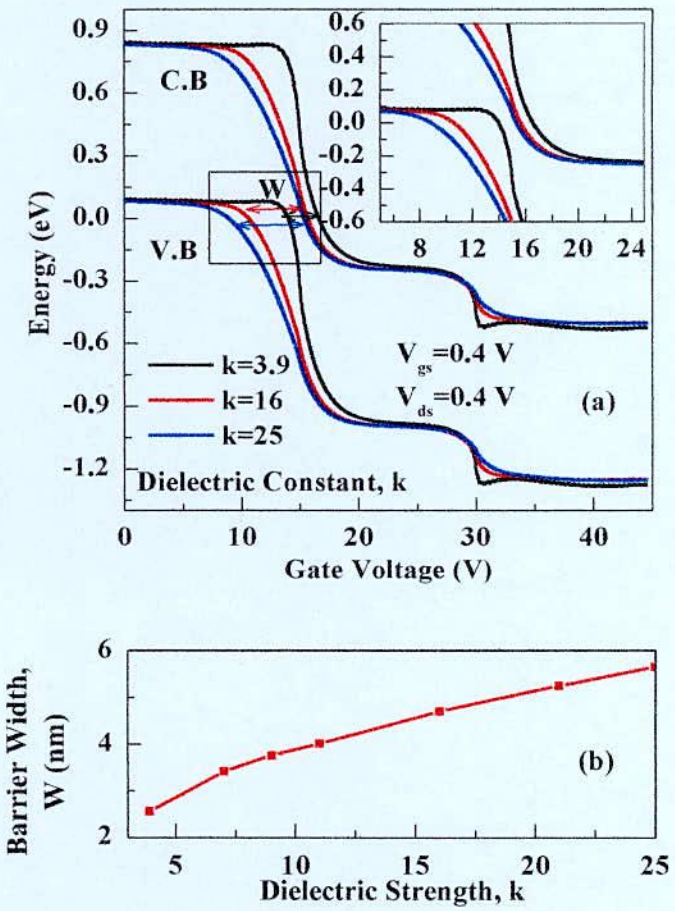

Figure 3.6: (a) ON state band diagram for k=3.9, k=16 and k=25(b) Dielectric strength dependent barrier width. The results are obtained for the oxide thickness of 2 nm.

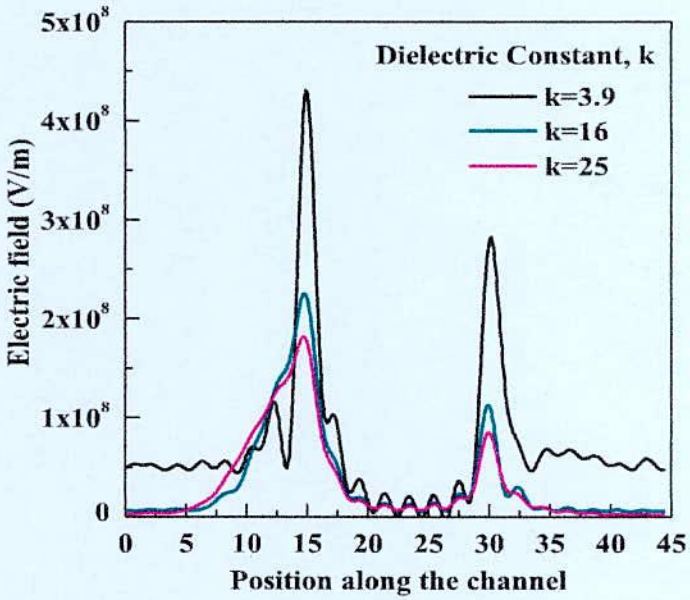

Figure 3.7: On state electric field distribution obtained for the oxide thickness of 2 nm for k=3.9, k=16 and k=25.

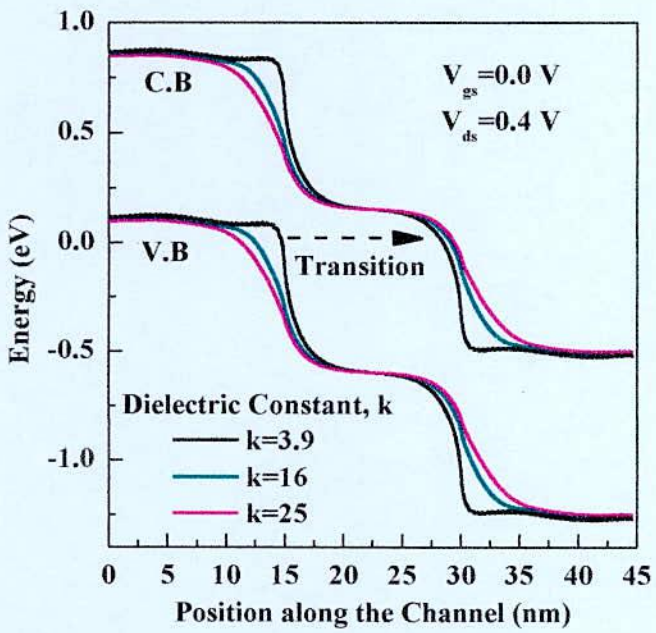

Figure 3.8: OFF state band diagram of OXESD CNT TFET structure for k=3.9, k=16 and k=25.

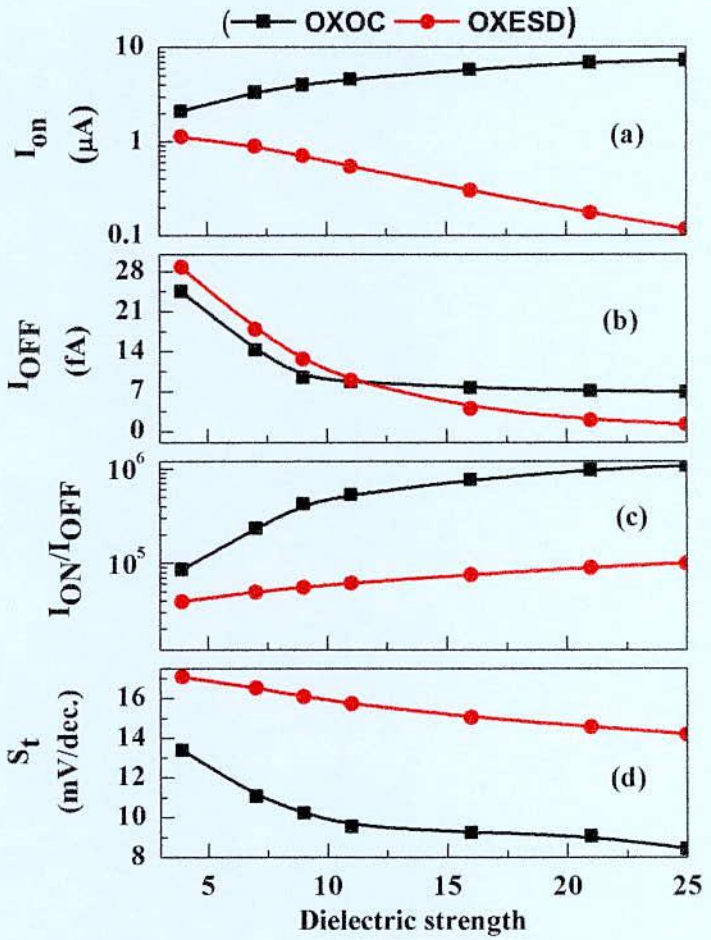

Figure 3.9: Dielectric strength dependent performance (a) I_{ON} (b) I_{OFF} (c) I_{ON}/I_{OFF} ratio (d) Subthreshold slope for OXOC and OXESD structure with oxide thickness of 2nm.

But for OXESD structure, in spite of having falling characteristics of both I_{ON} and I_{OFF}, shown in Fig.3.9 (a)" and Fig.3.9 (b) the I_{ON}/I_{OFF} ratio increases. This is because the reduction of I_{OFF} happens more significantly than the I_{ON} in their individual scale with the variation of oxide dielectric constants. So I_{ON}/I_{OFF} is found to be increased slowly for OXESD structure.

From the transfer characteristics we also found that the subthreshold slope of both of the devices decreases with increasing dielectric constant. The variation of subthreshold slope with dielectric constant is shown in Fig.3.9 (d). When the oxide dielectric constant increases, smaller

voltage is required to obtain certain amount of ON state current. Here it is also seen that for whole range of dielectric constants OXOC structure shows better performance than OXESD structure.

3.3 Gate oxide thickness dependent performnce

To study the gate oxide thickness dependent performance of the two proposed devices, we varied the oxide thickness from 0.5 nm to 5.0 nm with 0.5 nm interval for both of the devices. In this case SiO_2 is used as the gate oxide material. The device structures and other device parameters are kept same as before.

We see from Fig.3.10 (a) and Fig.3.10 (b) that the I_{ON} of both of the devices has falling trends with the increasing oxide thickness while I_{OFF} has rising trends for the similar variation of oxide thickness. The ON state band diagram of these devices for different gate oxide thickness shown in Fig.3.11 (a) and Fig.3.11 (b) also support the results. The overall performances of these two devices with gate oxide thickness are presented in Fig.3.12. The barrier width of both devices is found to be reduced with increase in oxide thickness. As a result the ON state current increases in both cases. The I_{ON}/I_{OFF} ratio of both devices reduces gradually with increase in oxide thickness. On the other hand, the subthreshold slope of both device increases with oxide thickness. So we can conclude that the overall performances of both of the device structures deteriorate with oxide thickness.

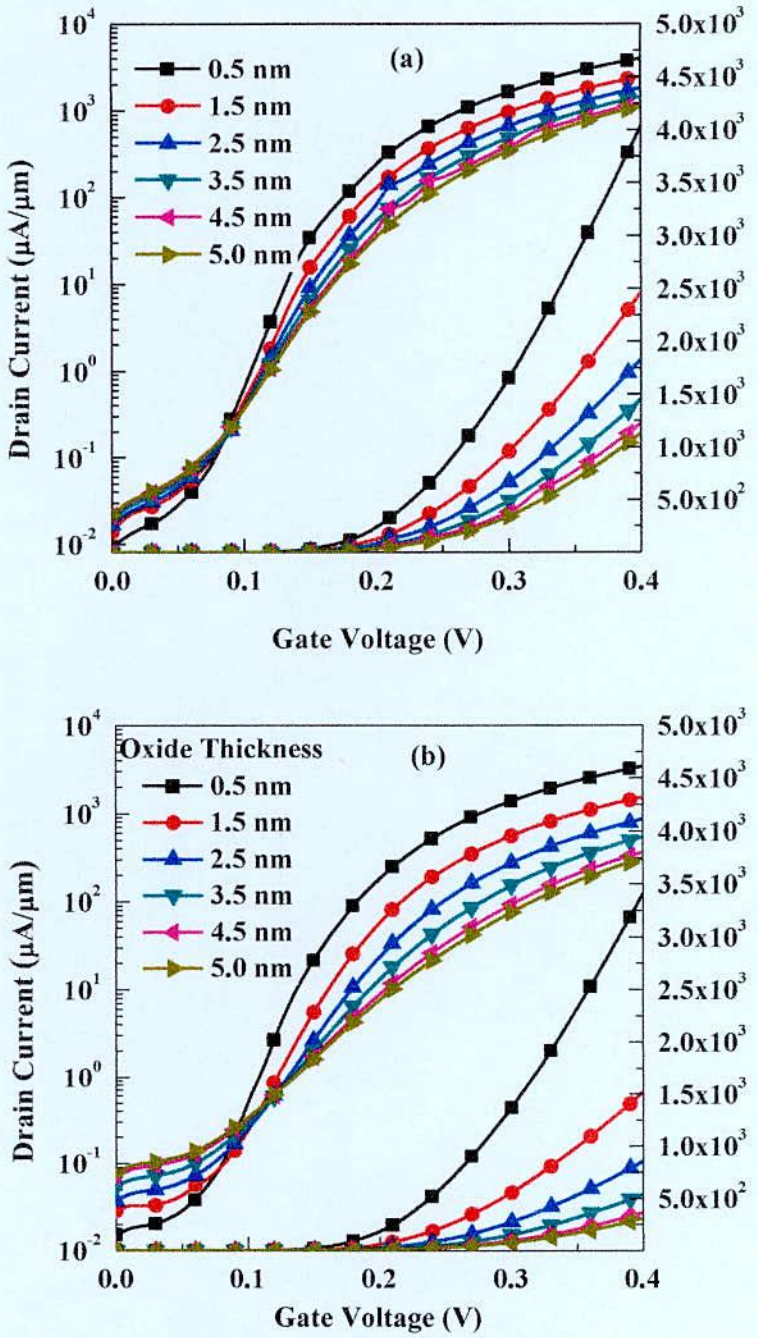

Figure 3.10: I_D-Vgs characteristics of (a) OXOC and (b) OXESD structures as a function of different gate oxide thicknesses. SiO2 (k=3.9) is used here as the gate oxide

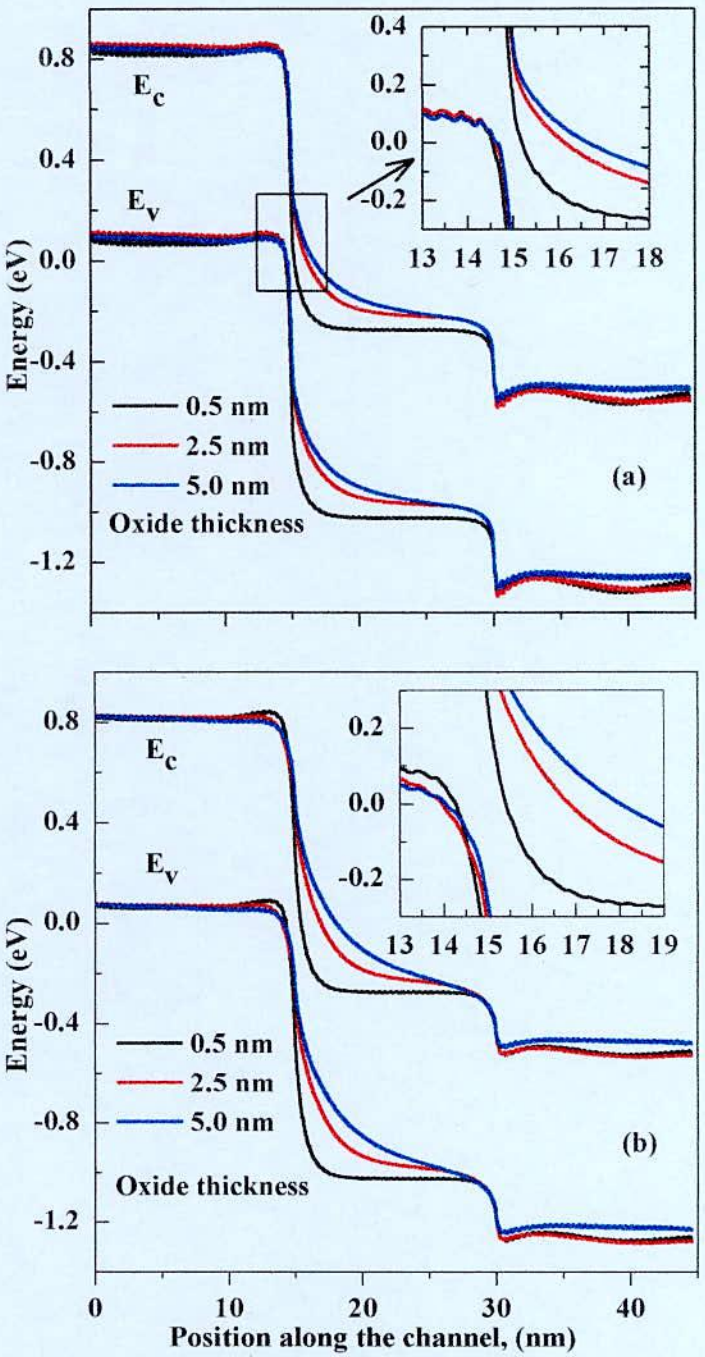

Figure 3.11: ON state band diagram of (a) OXOC and (b) OXESD structures as a function of different gate oxide thicknesses. SiO2(k=3.9) is used here as the gate oxide

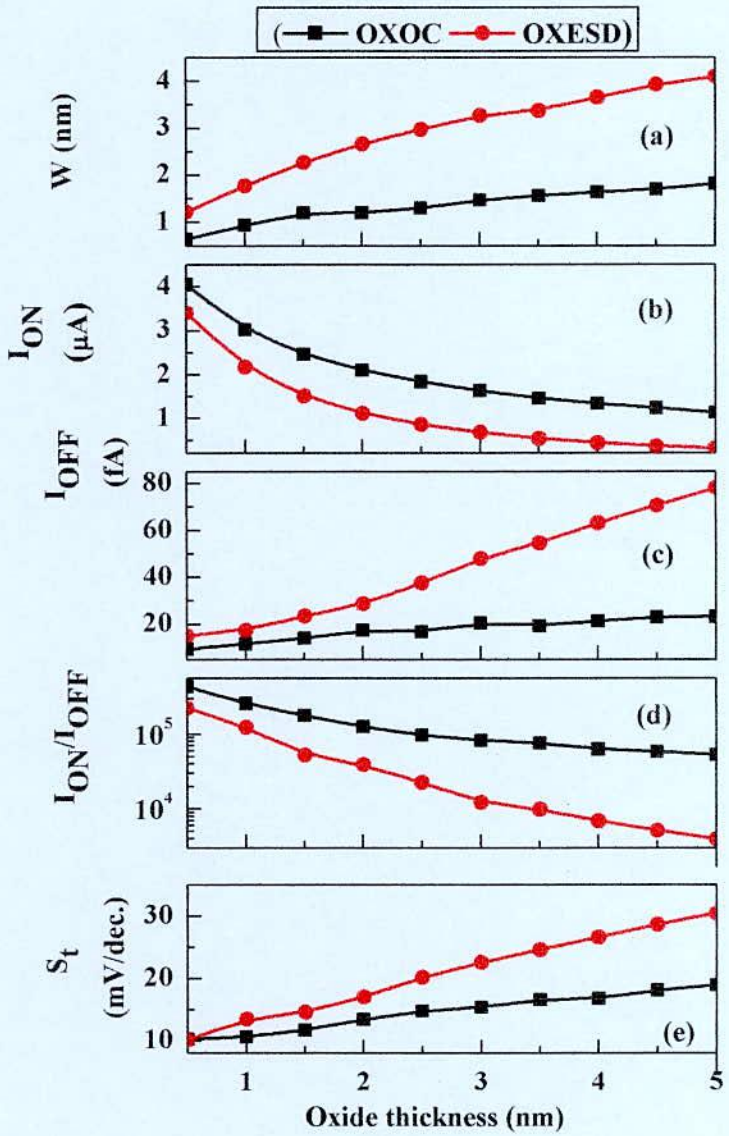

Figure 3.12: Gate oxide thickness dependent (a) barrier width (b) I_{ON} (c) I_{OFF} (d) I_{ON}/I_{OFF} ratio and (e) Subthreshold slope for the two proposed CNT TFET structures. The results are estimated for the gate oxide of SiO_2.

3.4 Channel length dependent performance

In this section of the thesis, the channel length scaling is carried out independently in order to isolate the impact of channel length scaling over the device performance. The transfer characteristics of the two proposed device structures are studied first for various channel lengths shown in Fig.3.13. Here solid lines indicate the results corresponding to OXOC structure while

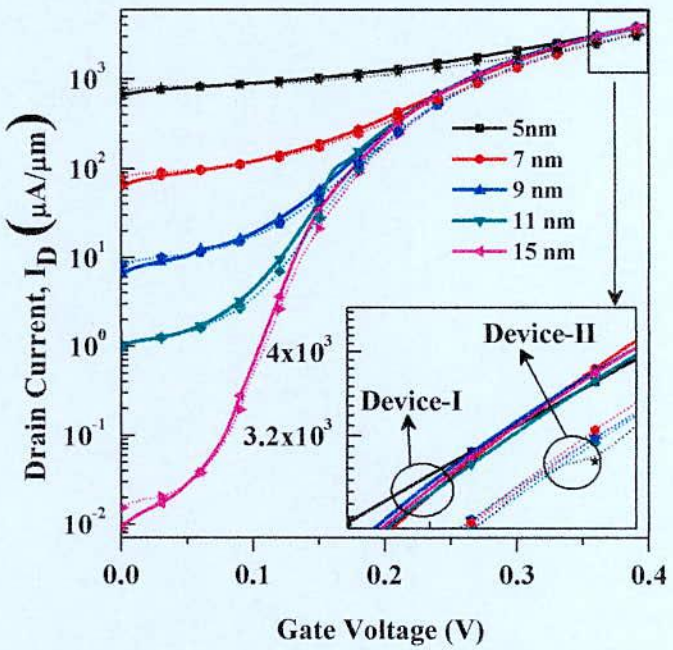

Figure 3.13: I_D-Vgs characteristics of OXOC (solid lines) and OXESD (dotted lines) structure as a function of channel length. Inset shows the extended view of ON state current corresponding to square marked region

the dotted lines corresponding to OXESD structure. It is found that for a particular channel length the performance of both of the devices follows a very close proximity especially at lower channel length. It is also found that the variation of ION with channel length for both of the devices is almost negligible (as shown in the inset of Fig.3.13), though IOFF varies significantly. Since the trend of variation is similar for both of the devices, the underlying physics is also expected to be similar. That is why we will explain the insight of the physics only once.

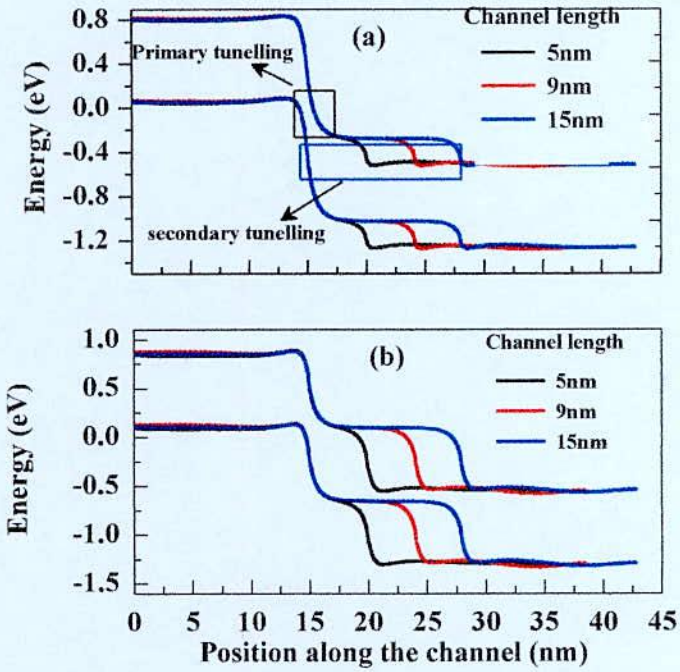

Figure 3.14: (a) ON state and (b) OFF state band diagram for different channel length.

In ON state band diagram shown in Fig.3.14 (a), it is seen that the primary tunneling region (indicated by black rectangle) and barrier width is almost constant for the variation of channel length. That is why, the I_{ON} is almost constant, though the minor variation occurs (shown in the inset of Fig.3.13) due to the change in tunneling distance in secondary tunneling region indicated by blue rectangle. The contribution of secondary tunneling current in ON state is quite negligible comparing the primary tunneling current. That is why the effect of channel length on ON state current of TFET is negligible.

But in OFF state the scenario is quite different, because here current is found only due to the secondary tunneling. For the OFF state band diagram shown in the in Fig.3.14 (b), it is seen that the tunneling distance in secondary tunneling region is gradually reduced with decrease in

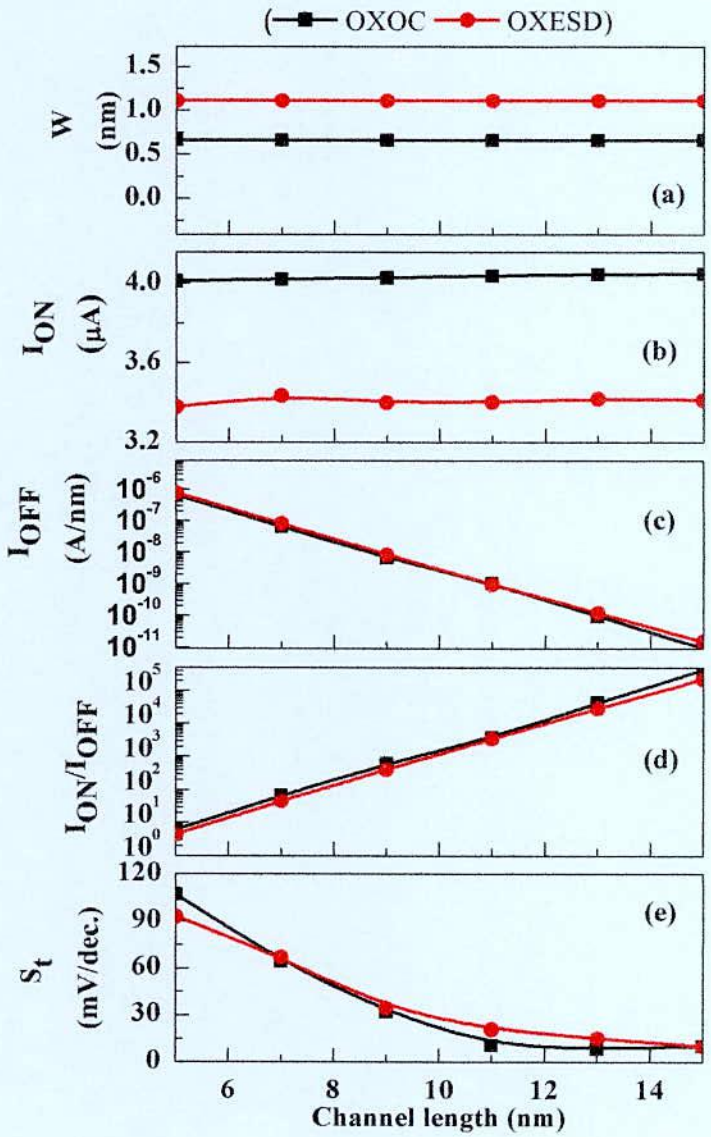

Figure 3.15: Channel length dependent (a) Barrier width (b) I_{ON} (c) I_{OFF} (d) I_{ON}/I_{OFF} ratio (e) Subthreshold slop of two proposed CNT TFET.

channel length because here tunneling distance is proportional to the channel length.. As a result, with decreasing the channel length, the tunneling probability rises significantly and very high current is found in the OFF state of the devices at lower channel length. The channel length dependent performance of the two proposed CNT TFET structures are summarized in Fig.3.15. Here it is seen that, in ON state, the barrier width is constant with the variation of channel length

for both devices and hence the I_{ON} is almost constants. I_{OFF} increases with decrease in channel length explained before. As a result the I_{ON}/I_{OFF} ratio of the two proposed devices falls with subsequent rise of subthreshold slope with decrease in channel length.

3.5 Gate underlap dependent performance

In this section we explore a very interesting effect that is gate underlap over the performance of TFET. The gate underlap means, leaving a portion of the channel uncovered by gate terminal and is shown in "Figs 2.2(a)" and "Figs 2.2(b)".

The transfer characteristics of the two devices with 2, 4 and 6 nm gate underlap are compared with that of a device with no underlap (i.e., for which the gate is exactly aligned with metallurgical source-channel junction) in Fig.3.16(a) and Fig.3.16(b). In both cases, we see that the presence of gate underlap deteriorates the performance (i.e., reduces I_{ON}, increases I_{OFF}) of the devices. The ON state band diagram of both devices clearly explain the increase of barrier width with increase of gate underlap. This in turns results in the gradual fall of tunneling probability at the tunneling junction. So the tunneling current is reduced. As the channel-gate underlap is increased in the device the ambipolarity in the OFF state condition is emerged. The presence of ambipolarity in the transfer characteristics is also considered as the deterioration in the performance of the device.

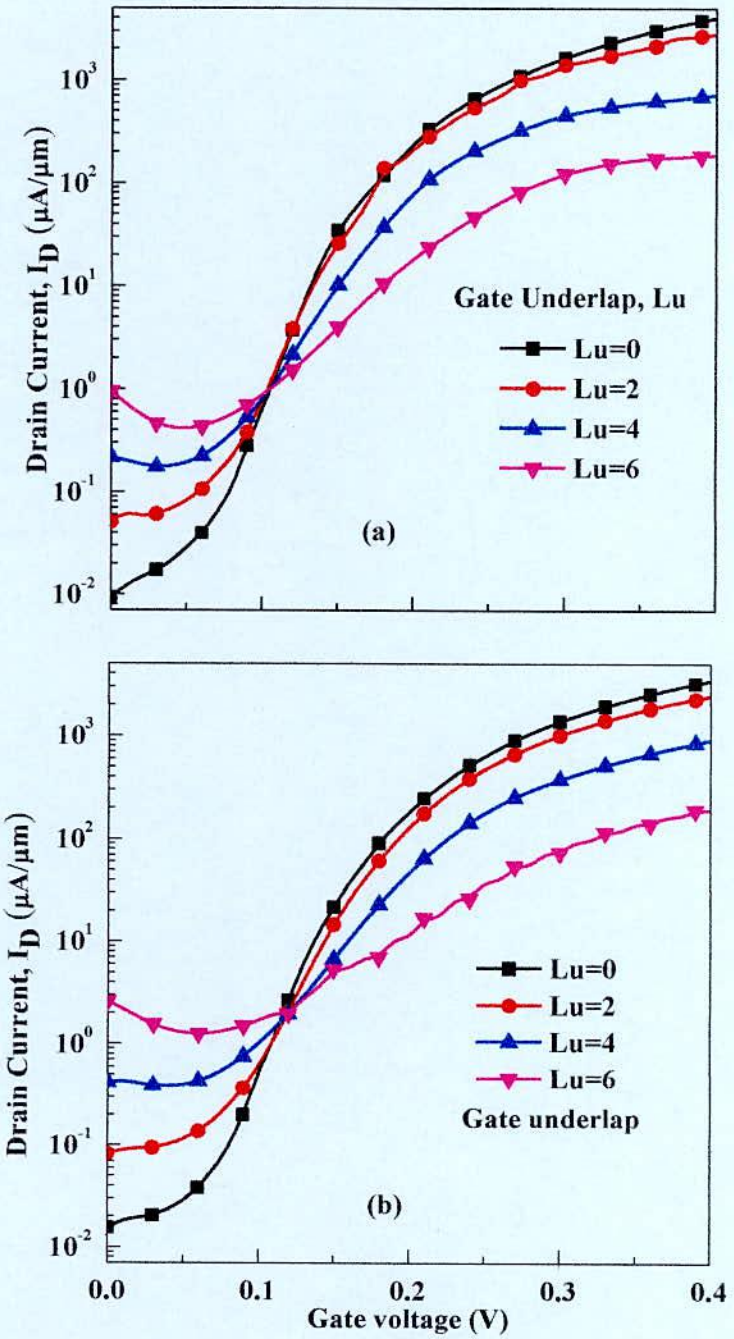

Figure 3.16: I_D-Vgs characteristics of (a) OXOC and (b) OXESD structures as a function of gate underlap.

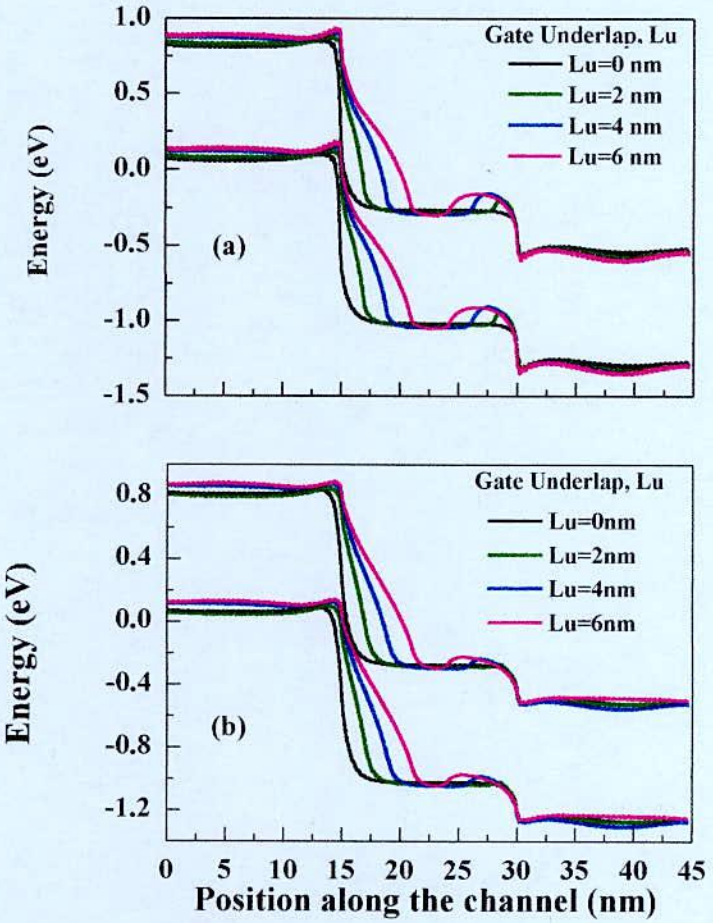

Figure 3.17: ON state band diagram of (a) OXOC and (b) OXESD structures as a function of gate underlap.

The overall performance of OXOC structure and OXESD structure under the effect of gate underlap is compared and summarized in Fig.3.18 shown below:

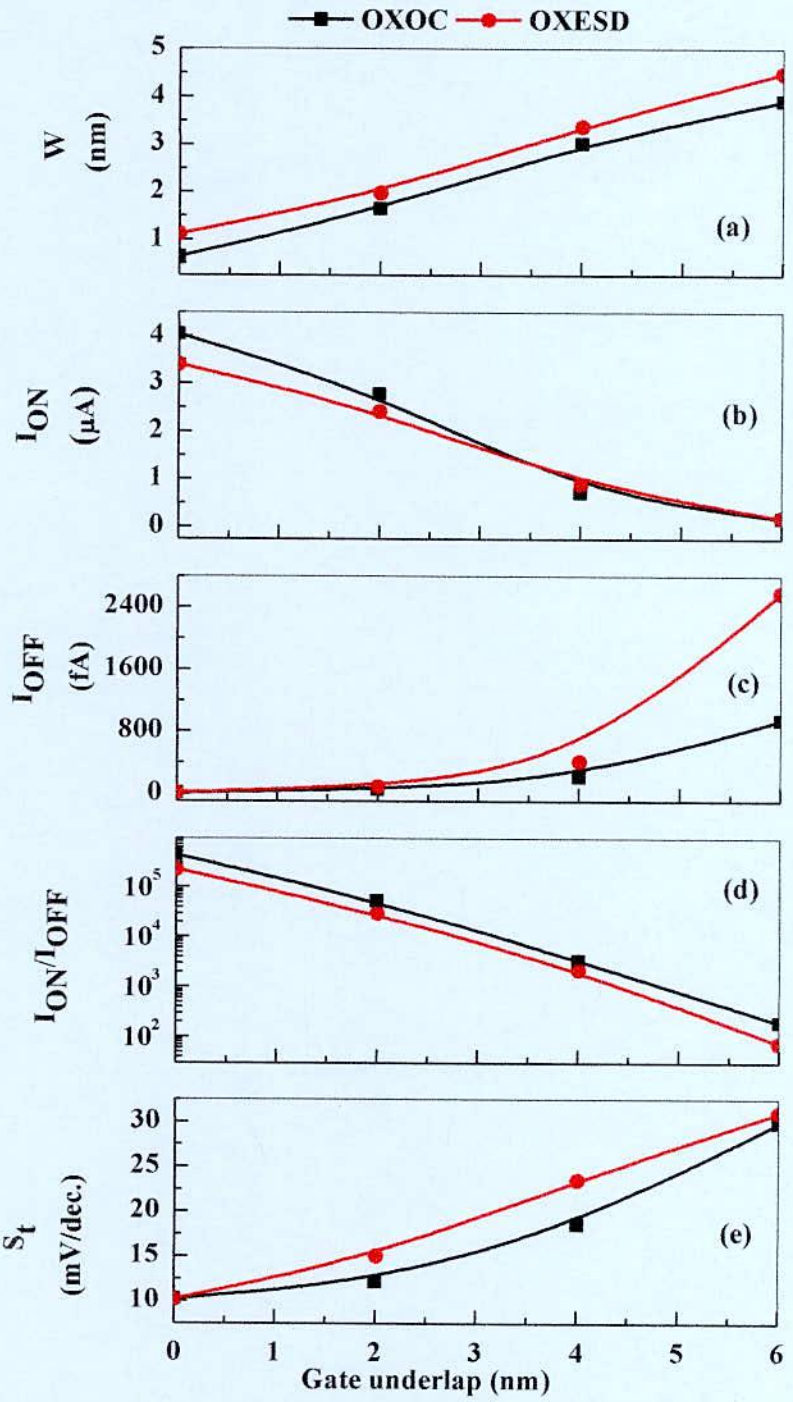

Figure 3.18: Gate underlap dependent (a) Barrier width (b) I_{ON} (c) I_{OFF} (d) I_{ON}/I_{OFF} ratio (e) Subthreshold slope of two proposed CNT TFET.

3.6 Doping concentration dependent performance

To study the impact of doping concentration (source-drain) on the performance of the

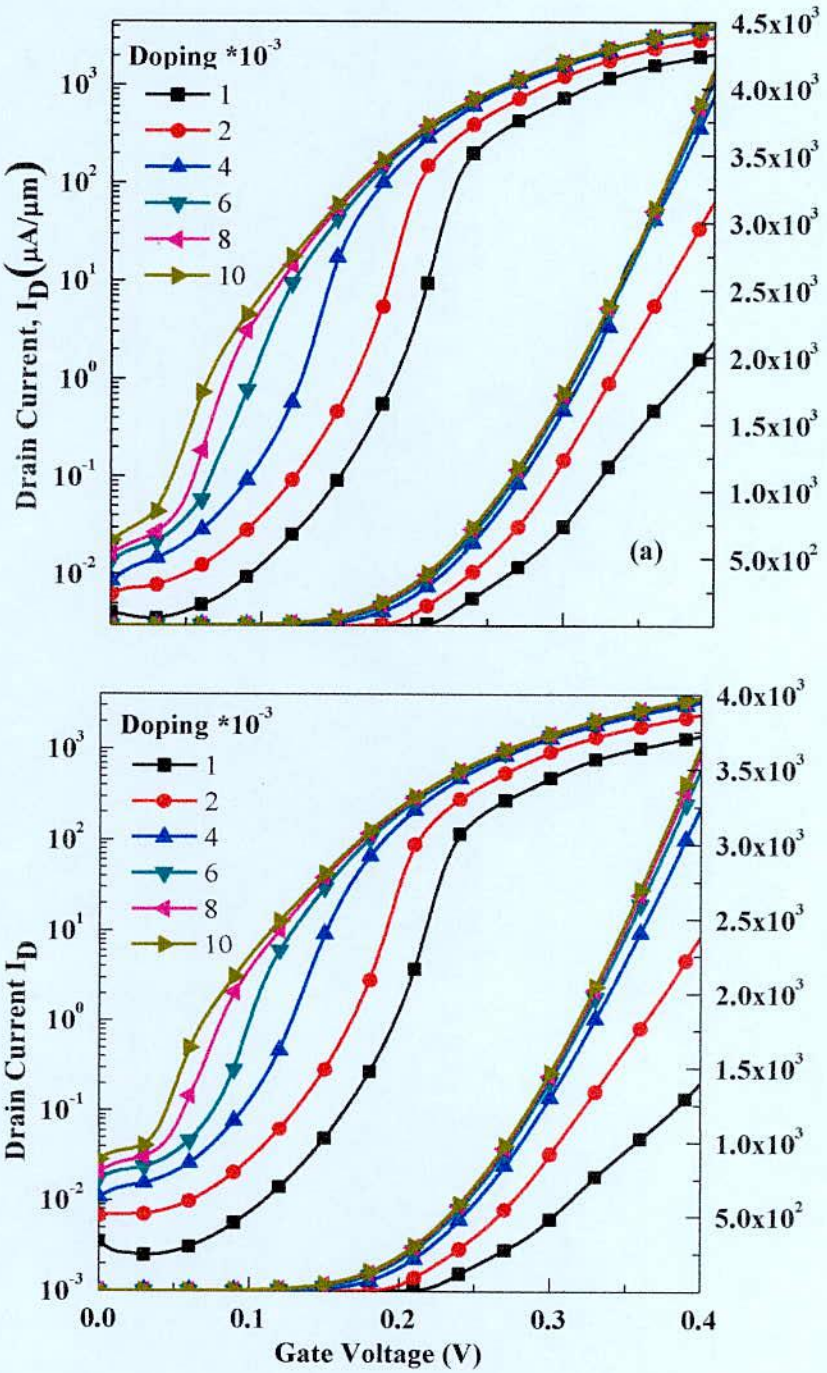

Figure 3.19: I_D-Vgs characteristics of (a) OXOC and (b) OXESD structures as a function of doping concentration.

devices, the devices are simulated under different doping concentration of 1, 2, 4, 6, 8, 10 × 10-3. It is seen that the threshold voltage of both devices shift significantly with doping concentration shown in Fig.3.19 (a) and in Fig. 3.19 (b).

It is also found that after doping concentration of 4×10^{-3}, further increase in doping concentration can make a very little (insignificant) change in the ON state current. This is because the barrier width becomes almost constant after 4×10^{-3} shown in "Fig.3.20 (a)". This leads to have almost constant ON state current as seen in "Fig.20 (b)". Although the ON current get saturated at a certain doping concentration the OFF current of both devices is observed to be increased with increase in doping concentration. So the I_{ON}/I_{OFF} ratio of both devices falls gradually with incresing doping concentration. Suthreshold slope of both devices is observed to be increases with increasing doping concentration shown in "Fig.3.20 (e)".

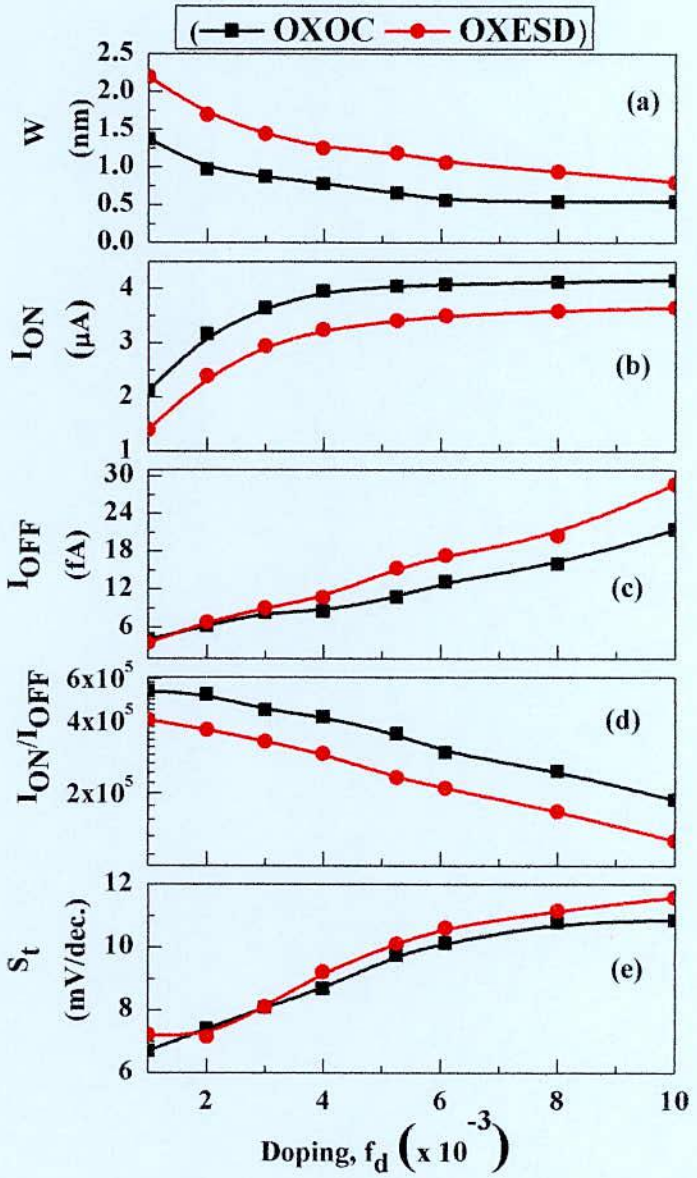

Figure 3.20: Doping concentration dependent (a) Barrier width, (b) I_{ON}, (c) I_{OFF}, (d) I_{ON}/I_{OFF} , ratio and (e) Subthreshold slop of two proposed CNT TFET.

3.7 Performance comparison between OXOC and OXESD structures in optimized condition

The main objective of this study is to find out the CNT TFET structure that gives the better performance. In order to do so, the I_D-V_G characteristics for both of the proposed deice structures are determined by optimizing the physical parameters of the devices. The gate oxide we used in optimized condition is HfO_2 of thickness 2.0 nm with dielectric constant of k=16 having equivalent oxide thickness (EOT) of 0.5 nm. The results are evaluated varying the gate bias V_{gs} from 0 to 0.4 V, while keeping the drain bias V_{ds} constants at 0.4 V. Other parameters such as doping concentration, channel length etc are mentioned in the table shown below:

Table 3.2: Optimized parameters used fordetermining the performance of OXOC and OXESD CNT TFET structures

Gate dielectric	HfO_2 with k=16
Oxide thickness	2 nm
Doping concentration, f_d	5×10^{-3}
Channel length	15 nm
Gate underlap, u_n	0

To compare the performance of these device structures we first present the transfer characteristics shown in Fig.3.21. The curves are plotted in both logarithmic and linear scales to understand the difference between I_{ON} and I_{OFF} clearly.

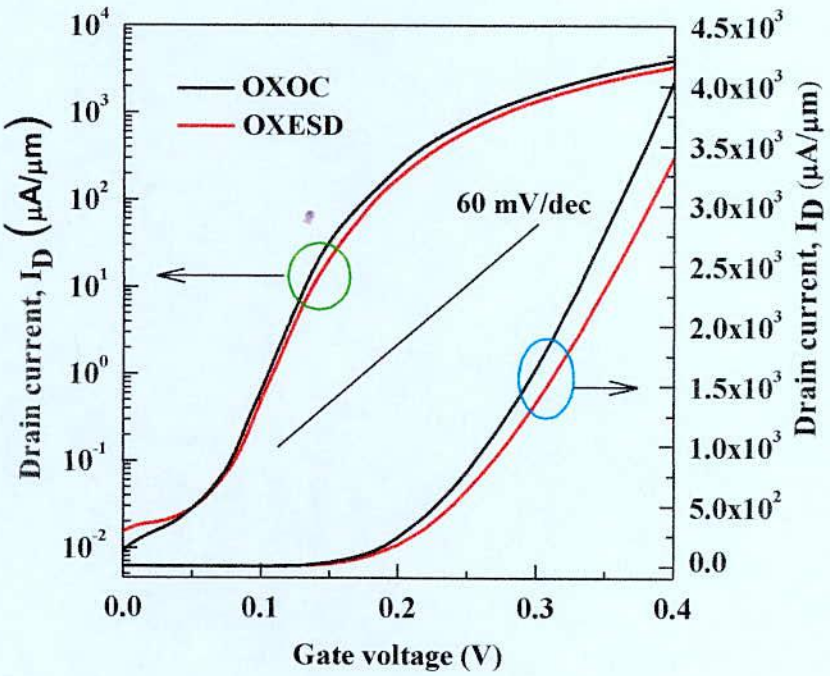

Figure 3.21: I_D-V_G characteristics of OXOC and OXESD structures under optimized condition.

It is found in Fig.3.21 that the OXOC structure provides higher ON state current than OXESD structure. The ON state currents for the OXOC and OXESD structures are estimated to be around 4046 μA/μm and 3412 μA/μm respectively, which are significantly better than those are reported earlier [][]. These results can be explained from the respective ON state band diagram and electric fields shown in Fig.3.22 and Fig.3.23. From the inset of ON state band diagram, it is seen that OXOC structure offer lower tunneling distance than the OXESD structure. As a result, the tunneling probability in OXOC becomes higher, which in turns results in higher ON state currents in OXOC structure than OXESD structure. The reason of getting higher currents in OXOC structure than OXESD structure can also be explained from their distribution of electric fields at the tunneling junction shown in Fig.3.23. Here it is found that the peak amplitude of the electric field at source to channel junction is higher for the OXOC than

OXESD structure. This electric fields is related to the transmission co-efficient of TFET by "eqn.2.4.6", which implies that, the higher electric fields results in higher transmission coefficient and finally higher ON state current. Therefore higher ON current is obtained from the OXOC than OXESD structure.

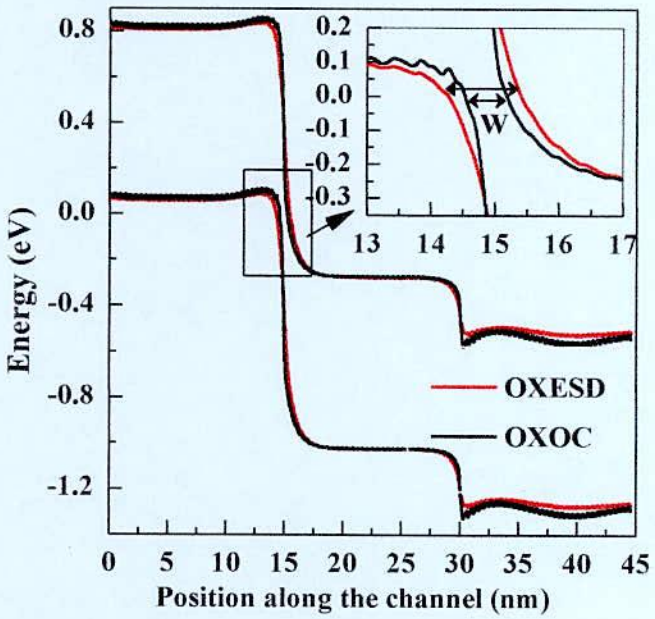

Figure 3.22: On state band diagram of OXOC and OXESD structures under optimized condition.

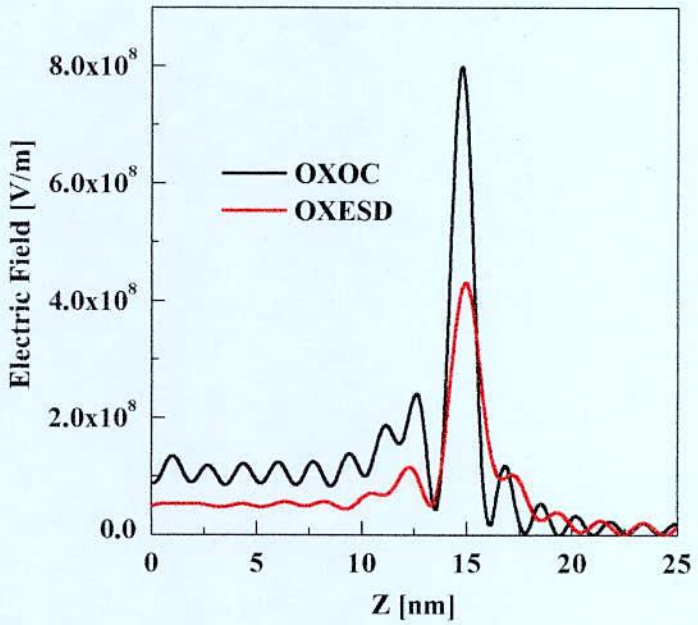

Figure 3.23: On state Electric fields at the source-channel junction of OXOC and OXESD structures under optimized condition

In the OFF state characteristics of the devices it is found that OXOC structure provides lower OFF state currents than OXESD structure, which can also be explained from the OFF state band diagram shown in Fig.3.24. Here the location of the highest electron transition (location of the lowest energy barrier) is represented by an arrow. It is seen from the extended view shown in the inset corresponding to the square marked region that the distance electrons need to travel for conduction from source to channel is larger in OXOC structure than OXESD structure. As a result tunneling probability in OXOC structure becomes smaller than OXESD structure in OFF state condition. As a result lower OFF current is found in OXOC structure than OXESD structure. From the transfer characteristics of these two devices it is clear that the OXOC structure results higher I_{ON}/I_{OFF} than OXESD structure. Again in OXOC structure the difference from ON to OFF state currents in the scale of currents is higher that the OXESD structure. That

means OXOC structure has sharper rising slop of current with respect to voltage, that is, smaller subthreshold slope is resulted in OXOC structure than OXESD structure, which indicates that lesser gate voltage is required to obtain a certain amount of drain current for the OXOC structure than the OXESD structure. The comparison of performance of these two devices is listed in the "Table-3.3".

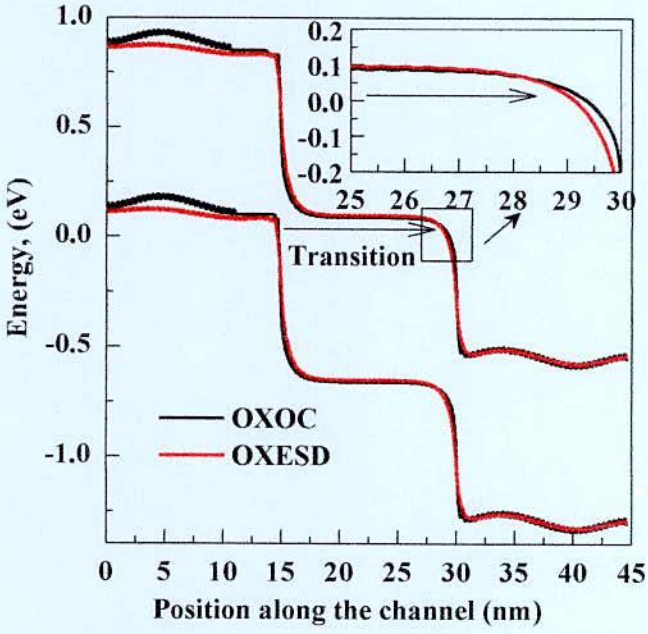

Figure 3.24: OFF state band diagram of OXOC and OXESD structures under optimized condition.

Table 3.3: Performance comparison of OXOC and OXESD structures under optimized condition

Performance parameter	OXOC structure	OXESD structure
ON state current, I_{ON} (μA/μm)	4046	3412
OFF state current, I_{OFF} (μA/μm)	0.0094	0.0153
I_{ON}/I_{OFF} ratio	4.3×10^5	2.2×10^5
Subthreshold slop, S_t (mV/dec)	10.19	10.37

Chapter 4 CONCLUDING REMARKS

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Chapter outlines

Conclusion

Suggestion for Future Works

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4.1 Conclussion

In this research work we presented two double gates CNT TFET structures: (i) Oxide only over the channel (OXOC) and (ii) Oxide extended over source to drain (OXESD). First the performance of these devices is explored under the variation of different device parameters including the dielectric strength, thickness of the gate oxide materials, channel length, doping concentration and gate underlap. And then to find out the better device structure the performances of the devices are studied under optimized condition. The transfer characteristics, on/off current (I_{ON}/I_{OFF}) ratio and subthreshold slope of the devices are investigated using Non Equilibrium Greens Function (NEGF) formalism in tight binding frameworks. The results are obtained by solving the NEGF and Poisson's equation self-consistently in NanoTCAD ViDES environment.

The results obtained from the simulation demonstrate that, in OXOC structure, gate oxide with higher dielectric constants enhances the I_{ON}, I_{OFF}, I_{ON}/I_{OFF} and subthreshold performance, but in case of OXESD the performance are found to deteriorate. While Changing oxide thickness the ION and ION/IOFF ratio found to decrease although the subthreshold slope and IOFF increases with oxide thickness. Since the higher dielectric constant oxide material with smaller thickness gives better results, we choose the HfO_2 with 2nm thickness (having EOT of 0.5nm) in order to have optimized gate oxide condition. The effect of channel length is further determined and found that the channel length have observed and found that channel length has has no significant impact on the ON state performance, although OFF state performance is highly influenced by channel length. To get a reasonable I_{ON}/I_{OFF} ratio, 15 nm is chosen as optimized channel length. The effect of gate channel underlap is also investigated and found that presence of underlap deteriorate the device performance. So the gate channel with zero underlap is considered as the optimized parameter. Furthermore the ON state current increases with doping

concentration and is found gets saturated for the doping concentration of 5×10^{-3}. If the doping density increases further, the OFF state current increases, which leads higher static power consumption and reduction of I_{ON}/I_{OFF} ratio. So 5×10^{-3} is considered as the optimized doping concentration. After having the optimized parameters the OXOC and OXESD device structures are simulated and compared. We found that under the optimized condition the OXOC shows the better performance than OXESD structures. The optimized ION, IOFF, ION/IOFF and subthreshold slope performances are found to be 4046 μA/μm, 0.0094 μA/μm, 4.3×10^{5} and 10.19 mV/decade respectively for the OXOC structure, which are significantly better results for the CNT based TFET so far reported previously.

4.2 Suggestion for Future Works

In this thesis we simulated CNT tunneling FET with gate length of 15 nm and in the gate we used single material. The future works related to this work can be extended on two point of view. One is structure and another is channel material. Since the performance of semiconductor devices are dependent on their structures, different structures can be studied including planner gate al-around (GAA), Planner single gate e.t.c for further reduction of OFF state current..

On the other other-hand some emerging 2-D material including silicene, WS_2, MoS_2, phosphorene can be used as the channel material and investigate their prospect for the tunneling FET.

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