Design and Implementation of Sampling Rate Conversion System for Electroencephalogram (EEG) on FPGA Device

by

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A project submitted in partial fulfillment of the requirements for the degree of Master of Engineering in Electronics and Communication Engineering

Khulna University of Engineering & Technology
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November, 2018

Declaration

This is to certify that the project work entitled *"Design and Implementation of Sampling Rate Conversion System for Electroencephalogram (EEG) on FPGA Device"* has been carried out by *Mahamudul Hassan* in the Department of *Electronics and Communication Engineering*, Khulna University of Engineering & Technology (KUET), Khulna, Bangladesh. The above project work or any part of this work has not been submitted anywhere for the award of any degree or diploma.

Signature of Supervisor

Signature of Candidate

Approval

This is to certify that the project work submitted by *Mahamudul Hassan* entitled *"Design and Implementation of Sampling Rate Conversion System for Electroencephalogram (EEG) on FPGA Device"* has been approved by the board of examiners for the partial fulfillment of the requirements for the degree of *M. Sc. Engineering (M. Sc. Eng.)* in the Department of *Electronics and Communication Engineering*, Khulna University of Engineering & Technology (KUET), Khulna, Bangladesh in November, 2018.

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Acknowledgment

With due respect and honor, I want to express my gratitude to Almighty Allah. I express my indebtedness to my dedicated supervisor Dr. Sheikh Md. Rabiul Islam (Professor, Department of Electronics and Communication Engineering, KUET) for his necessary guidance, suggestions and encouragement to all phases of my work. I would also like to thank all the teachers who've been much helpful and encouraging in completion of our project work.

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Abstract

The wide scale use of digital communication and digital media has made the necessity of methods to process digital data more important now-a-days. The signal-rate system in digital signal processing has evolved the key of fastest speed in digital signal processor. Field Programmable Gate Array (FPGA) offers good solution for addressing the needs of high-performance DSP systems. This concept leads to a chip with attractive features like, low requirements for the coefficient word lengths, significant saving in computation and storage requirements results in a significant reduction in its dynamic power consumption. There are many algorithms have been proposed for processing of biomedical signal. Main objectives of these algorithm are to minimize noise and artifacts existing with these signals, so that it will be easy to analyze and diagnosis human diseases. The proposed system has many advantages on signal processing such that it has a simple structure, stationary response and adaptively with embedded microprocessors. The system is proposed due to facilitate structural characteristic and design properties on filtering EEG signal. The focus of this project is on the basic DSP functions, namely filtering signals to remove unwanted frequency using Sampling Rate Conversion (SRC) in digital signal processing. The system has a computer where the design can be programmed and simulated on Xilinx® Integrated Software Environment (ISE) Suite 14.7 or Quartus II software with interface ALTRA Cyclone DE II board of FPGA device.

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   http://iaset.us/view_archives.php

2. **Mahamudul Hassan**, Sheikh Md. Rabiul Islam, "Design and Implementation of Pre-processing Chip for Brain Computer Interface Machine," *International Conference on Robotics, Electrical and Signal Processing Techniques 2019* (ICREST 2019), January 10-12, 2019, American International University Bangladesh (AIUB), Dhaka, Bangladesh. [Accepted]

CHAPTER I

Introduction

Chapter Outlines

- Introduction
- Motivation
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CHAPTER 1

Introduction

1.1 Introduction

Electroencephalogram (EEG) is a signal with electrical activities for the study of human cognition states. The measurement of these electrical activities can be taken from standardized channel; locations on the scalps [1.1]. The EEG signal contains noises and artifacts during the recording of the EEG signal. The noise from the main source like electrooculogram (EOG), electrocardiogram (ECG), electromyogram (EMG) and other sources should be eliminated to increase accuracy of EEG signal processing in bio-chip system. However, it may produce less accurate results than the software processing because of the appearance of quantization errors [1.4-1.5].

The most of bio-system has got physiological artifacts due to the variety of body activities such as body movements, skin resistance fluctuations or other bioelectrical potentials. From this aspect researcher raise the question how to develop digital filter chip to remove these artifacts. The FPGA is employed in the analysis of EEGs in this project to perform smooth EEG signal based on the proposed sampling rate conversion system. The proposed system works with sampling rate conversion for high speed data and lower time resolution. The main approach of this system is to change the sampling rate of the EEG signals and convert it back into analog and then to re-digitize it at a new rate. The quantization and aliasing errors inherent in digital-analog-digital conversion processing, would degrade the signal. In this project uses Sample Rate Conversion (SRC) for changing the sampling frequency of a signal digitally. Its main attraction is that if allows the strengths of a conventional DSP to be exploited. For example, much of the anti-aliasing and anti-imaging filtering in real-time DSP systems can be performed in the digital domain, enabling both sharp magnitude frequency as well as phase responses to be achieved.

1.2 Motivation

In this project proposed Sampling Rate Conversion (SRC) System has designed due to some limitations of traditional DSP system. This system will remove noise and artifacts of EEG signal which are collected from the scalp of human. This concept leads to a chip with attractive features like, low requirements for the coefficient word lengths, significant saving in computation and storage requirements results in a significant reduction in its dynamic power consumption**.**

This project is also to present a Field Programmable Gate Array (FPGA)-based proposed digital filter design using sampling rate conversion for biomedical signal processing. The proposed system has many advantages on signal processing such that it has a simple structure, stationary response and adaptively with embedded microprocessors. Another important advantage to FPGA to digital filter implementation include higher sampling rate as compared to traditional DSP chips. This concept can be used in Brain Computer Interface (BCI) system.

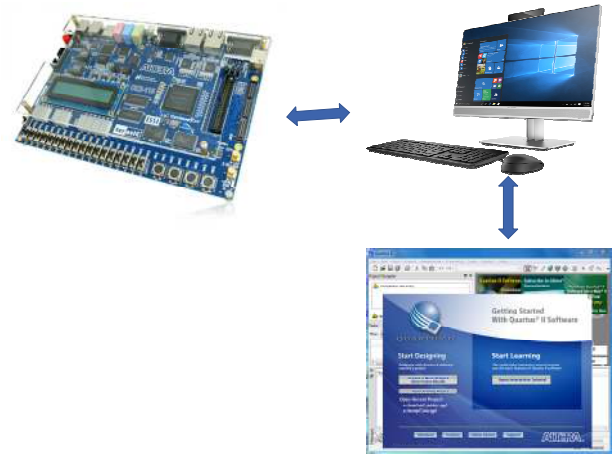

Figure 1.1: Work flow diagram of this project.

Figure 1.1 shows the relationship between computer, ALTERA DE2 board and Quartus II prime software. Proposed system design can be programmed and simulated on Xilinx[@] Integrated Software Environment (ISE) Suite 14.7 or Quartus II software installed within the computer with interface ALTRA Cyclone DE II board of FPGA device [1.13].

1.3 Problem Statement

Mostly EEG-based brain-computer interface (BCI) systems that are being developed focus on novel pre-processing filtering, feature extraction algorithms, classification methods and combining existing approaches to create hybrid BCIs [1.1]. This hybrid BCI showed on improve accuracy for data acquisition. But still, BCI systems are far from realization for daily use. Due to noise and artifact into BCI system lost potential to improve accuracy. Proper filters need to be designed to filter these artifacts. From this aspect researcher raise the question how to develop digital filter chip to remove these artifacts**.** The FPGA is employed in the analysis of EEGs in this project to perform smooth EEG signal based on the proposed sampling rate conversion system**.**

Many Algorithms and techniques have been developed to remove noise and artifacts from EEG signal those are collected from the scalp of human. Others techniques like ASIC, Microcontroller etc. have some disadvantages over FPGAs. FPGAs are designed in such a way that it can perform both analog and mixed signal. ASIC are full custom so that they require higher development cost to design and implement as compared to FPGAs. ASIC are not reprogrammable for that any kind of changes requires cost again. ASIC design tools are also expensive so you have to expense huge amount of NRE. Some large ASICs can take a year or more to design.

Considering these drawbacks of ASICs over FPGAs. Most engineers and IC production industries are like to use FPGAs to design digital filter to remove noise and artifacts from EEG signal. In this project, FPGA techniques are used to design and implement a filter that can remove noise and artifacts from EEG signals and delivery the actual signal those comes from the scalp of human. Some researchers have done different methods for filter design as review, references [1.2-1.4], [1.7-1.13] use Xilinx chips; [1.14] Altera devices; both Xilinx and Altera; [1.12] both Orca and Xilinx; and uses CLI [1.13].

1.4 Review of Related Research Work on Project

Filter adds more noise to signal; the digital filter performs noiseless mathematical operations at each intermediate step in the transform [1.10]. According to the digital filter has merge as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architecture. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain

with analog filters. FIR and IIR filters are the two common filter forms. The creation and analysis of representative data can be a complex task. Most of the filter algorithms require multiplication and addition in real-time. The unit carrying out this function is called MAC (multiply accumulate). Depends on how good the MAC is, the better MAC the better performance can be obtained.

The most common approaches to the implementation of digital filtering algorithms are general purpose digital signal processing chips for audio applications, or special purpose digital filtering chips and application-specific integrated circuits (ASICs) for higher rates [1.11]. An approach to the implementation of digital filter algorithms on field programmable gate arrays (FPGAs). Recent advances in FPGA technology have enabled these devices to be applied to a variety of applications traditionally reserved for ASICs. FPGAs are well suited to data path designs, such as those encountered in digital filtering applications. The density of the new programmable devices is such that a nontrivial number of arithmetic operations such as those encountered in digital filtering may be implemented on a single device. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches. Lack of flexibility can forestall the cost-effective evaluation of exotic algorithms in a high-performance real-time environment. Only high-volume applications or extremely critical low volume applications can justify the expense of developing a full custom solution. There are a variety of algorithms which are not within the performance envelope of general-purpose processors, and which are not sufficiently commonplace or well-understood to justify implementation in a full custom design.

Field programmable gate arrays (FPGAs) can be used to alleviate some of the problems with the custom approach. FPGAs are programmable logic devices which bear a significant resemblance to traditional custom gate arrays. FPGAs are in-system programmable, which allows the modification of the operation of the device through simple reprogramming. Electroencephalography (EEG) is a technique of observing and monitoring human brain activity by electrical mean. Human brain produces very small amount of electrically measurable waves. EEG recording includes noises and artifacts from various sources which can cause serious difficulties and remarkable problems in EEG data analysis. Most common artifacts are caused by inappropriate electrode positioning, improper equipment setup etc. These are the technical artifact

and there are also some physiological artifacts resulted from the biological signals.

In recent years, independent component analysis (ICA) has been proved as a powerful algorithm to solve blind source separation (BSS) problems in a variety of signal processing. Applications such as speech, image, or biomedical signal processing. Especially biomedical signals, which are different signal sources from organs such as brain, heart, or muscles, push the ICA algorithm to process more channels than speech or image applications. However, the characteristic of general ICAs is limited to only process off-line and enormous data [1.13]. On clinic, this cannot assist doctors in real-time diagnosis. Thus, more researches focus on other reliable equipment from points of view on software or hardware implementation.

1.5 Objectives

The major objectives of this project are as follows:

- To design Sampling Rate Conversion System for EEG signal.
- To design algorithm for Sampling Rate Conversion system and analysis the result of Sampling Rate Conversion system.
- Analyze the timing diagram of the SRC system.
- Verify the output result of Xilinx or Quartus II with ALTERA Cyclone DE II board of FPGA device.

1.6 Project Organization

This section provides a summary of all the chapters covered in this project.

Chapter 1: This chapter describes the introduction to the project, the problem description, motivation of this system and objective.

Chapter 2: This chapter describes the basic concept of EEG signal, classifications of EEG signal, analysis of EEG signal, Field Programmable Gate Array (FPGA) Technology, ALTERA FPGA DE II, internal structure of Cyclone DE II FPGA chip, and some basic concept of the design platform Xilinx.

Chapter 3: This chapter will describe the methodology for Method I, Sampling Rate Conversion System Method algorithm, analysis the RTL diagram and Timing diagram and finally discuss output of the proposed method I.

Chapter 4: This chapter will describe methodology for Method II, Sampling Rate Conversion System algorithm, analysis the RTL diagram and Timing diagram and finally discuss output of the proposed method II.

Chapter 5: This chapter will describe conclusion and future work.

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CHAPTER II

EEG Signal and FPGA Technology

Chapter Outlines

- Electroencephalogram (EEG)
- Field Programmable Gate Array (FPGA)
- Summary
- References

CHAPTER II

EEG Signal and FPGA Technology

2.1 Electroencephalogram (EEG)

2.1.1 Introduction

Electroencephalography is a medical imaging technique that reads scalp electrical activity generated by brain. The electroencephalogram (EEG) is defined as electrical activity of an alternating type recorded from the scalp surface after being picked up by metal electrodes and conductive media [2.2]. The EEG measured directly from the cortical surface is called electrocardiogram while when using depth probes, it is called electrogram. In this project, we will refer only to EEG measured from the head surface. Thus, electroencephalographic reading is a completely non-invasive procedure that can be applied repeatedly to patients, normal adults, and children with virtually no risk or limitation. When brain cells are activated, local current flows are produced. EEG measures mostly the currents that flow during synaptic excitations of the dendrites of many pyramidal neurons in the cerebral cortex. Differences of electrical potentials are caused by summed postsynaptic graded potentials from pyramidal cells that create electrical dipoles between soma (body of neuron) and apical dendrites (neural branches). Brain electrical current consists mostly of Na+, K+, Ca++, and Cl- ions that are pumped through channels in neuron membranes in the direction governed by membrane potential [2.3]. The detailed microscopic picture is more sophisticated, including different types of synapses involving variety of neurotransmitters. Only large populations of active neurons can generate electrical activity recordable on the head surface. Between electrode and neuronal layers current penetrates through skin, skull and several other layers. Weak electrical signals detected by the scalp electrodes are massively amplified, and then displayed on paper or stored to computer memory [2.4]. Due to capability to reflect both the normal and abnormal electrical activity of the brain, EEG has been found to be a very powerful tool in the field of neurology and clinical neurophysiology. The human brain electric activity starts around the 17-23 week of prenatal development. It is assumed that at

birth the full number of neural cells is already developed, roughly 1011 neurons [2.5]. This makes an average density of 104 neurons per cubic mm. Neurons are mutually connected into neural nets through synapses. Adults have about 500 trillion (5.1014) synapses. The number of synapses per one neuron with age increases, however the number of neurons with age decreases, thus the total number of synapses decreases with age too. From the anatomical point of view, the brain can be divided into three sections: cerebrum, cerebellum, and brain stem. The cerebrum consists of left and right hemisphere with highly convoluted surface layer called cerebral cortex. The cortex is a 1 Measurement in Biomedicine M. Teplan dominant part of the central nervous system. The cerebrum obtains centers for movement initiation, conscious awareness of sensation, complex analysis, and expression of emotions and behavior. The cerebellum coordinates voluntary movements of muscles and balance maintaining. The brain stem controls respiration, heart regulation, biorhythms, necrohormone and hormone secretion, etc. [2.6]. The highest influence to EEG comes from electric activity of cerebral cortex due to its surface position. There are some theoretical and practical differences between EEG and MEG. Although the MEG is produced by the same electrical currents, it can provide complementary information to EEG [2.7].

2.1.2 History of EEG

During more than 100 years of its history, encephalography has undergone massive progress. The existence of electrical currents in the brain was discovered in 1875 by an English physician Richard Caton. Caton observed the EEG from the exposed brains of rabbits and monkeys. In 1924 Hans Berger, a German neurologist, used his ordinary radio equipment to amplify the brain's electrical activity measured on the human scalp. He announced that weak electric currents generated in the brain can be recorded without opening the skull, and depicted graphically on a strip of paper. The activity that he observed changed according to the functional status of the brain, such as in sleep, anesthesia, lack of oxygen and in certain neural diseases, such as in epilepsy. Berger laid the foundations for many of the present applications of electroencephalography. He also used the word electroencephalogram as the first for describing brain electric potentials in humans. He was right with his suggestion that brain activity changes in a consistent and recognizable way when the general status of the subject changes, as from relaxation to alertness [2.2]. Later in 1934 Adrian and Matthews published the paper verifying concept of “human brain waves” and identified regular oscillations around 10 to 12 Hz which they termed “alpha rhythm” [2.3].

2.1.3 Use of EEG Signal

EEG signal is used to detect electrical activity of brain. This signal can be used to find different disorders like

I. Seizure Disorder
II. Head Injury
III. Encephalitis (Inflammation of Brain)
IV. Brain Tumor
V. Encephalopathy (disease that causes brain dysfunction)
VI. Sleep Disorder
VII. Stroke

2.1.4 Classification of EEG Signal

EEG signal can be classified into four [2.1] different categories. Figure 2.1 shows the classifications of EEG signal with their waveform. These are:-

1. Delta
2. Theta
3. Alpha
4. Beta

Delta: has a frequency of 3 Hz or below. It tends to be the highest in amplitude and the slowest waves. It is normal as the dominant rhythm in infants up to one year and in stages 3 and 4 of sleep. It may occur focally with subcortical lesions and in general distribution with diffuse lesions, metabolic encephalopathy hydrocephalus or deep midline lesions. It is usually most prominent frontally in adults (e.g. FIRDA - Frontal Intermittent Rhythmic Delta) and posteriorly in children e.g. OIRDA - Occipital Intermittent Rhythmic Delta).

Theta: has a frequency of 3.5 to 7.5 Hz and is classified as "slow" activity. It is perfectly normal in children up to 13 years and in sleep but abnormal in awake adults. It can be seen as a manifestation of focal subcortical lesions; it can also be seen in generalized distribution in diffuse disorders such as metabolic encephalopathy or some instances of hydrocephalus.

Alpha: has a frequency between 7.5 and 13 Hz. It is usually best seen in the posterior regions of the head on each side, being higher in amplitude on the dominant side. It appears when closing the

eyes and relaxing, and disappears when opening the eyes or alerting by any mechanism (thinking, calculating). It is the major rhythm seen in normal relaxed adults. It is present during most of life especially after the thirteenth year.

Beta: beta activity is "fast" activity. It has a frequency of 14 and greater Hz. It is usually seen on both sides in symmetrical distribution and is most evident frontally. It may be absent or reduced in areas of cortical damage. It is generally regarded as a normal rhythm. It is the dominant rhythm in patients who are alert or anxious or have their eyes open.

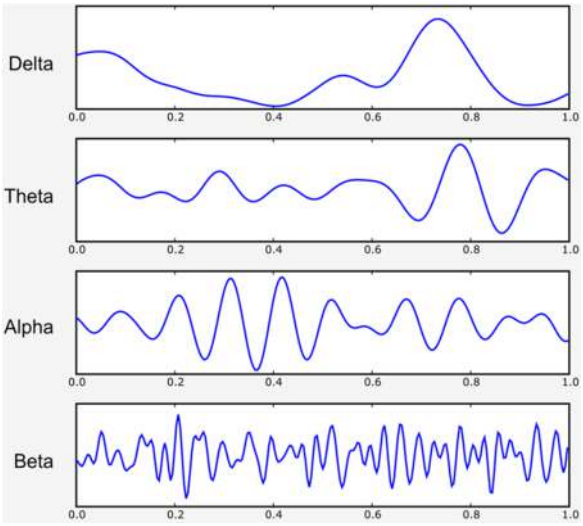

Figure 2.1: EEG Signal Classification.

2.1.5 Electroencephalogram (EEG) Signal Analysis

EEG analysis would also support the research an intelligent robot and assisted tools for the disabled. The study has been found to be time consuming, tedious and inefficient. Application of digital processing techniques to the recorded data or real time data results in helping the neurologist in speedy and accurate diagnosis in addition to data compression and ease of transmission for remote diagnosis. These techniques help in reviewing the records quickly, reduce human error making the expert neurologists' services available to a larger populace.

The EEG consists of a set of multi-channel signals. The pattern of changes in signals reflects large-scale brain activities. In addition, the EEG also reflects activation of the head musculature, eye movements, interference from nearby electric devices, and changing conductivity in the electrodes due to the movements of the subject or physicochemical reactions at the electrode sites. All of

these activities that are not directly related to the current cognitive processing of the subject are collectively referred to as background activities below. Formerly the problem with the interferences of other electric devices was solved by A Faraday cage which is an enclosure formed by conducting material, or by a mesh of such material. Such an enclosure blocks out external static electrical fields.

The EEG consists of a set of multi-channel signals. The pattern of changes in signals reflects large-scale brain activities. In addition, the EEG also reflects activation of the head musculature, eye movements, interference from nearby electric devices, and changing conductivity in the electrodes due to the movements of the subject or physicochemical reactions at the electrode sites. All of these activities that are not directly related to the current cognitive processing of the subject are collectively referred to as background activities below. Formerly the problem with the interferences of other electric devices was solved by A Faraday cage which is an enclosure formed by conducting material, or by a mesh of such material. Such an enclosure blocks out external static electrical fields. But this realization proved to be expensive and digital filtration is preferred now. Figure 2.2 shows the electrode placement on scalp for recording EEG signal.

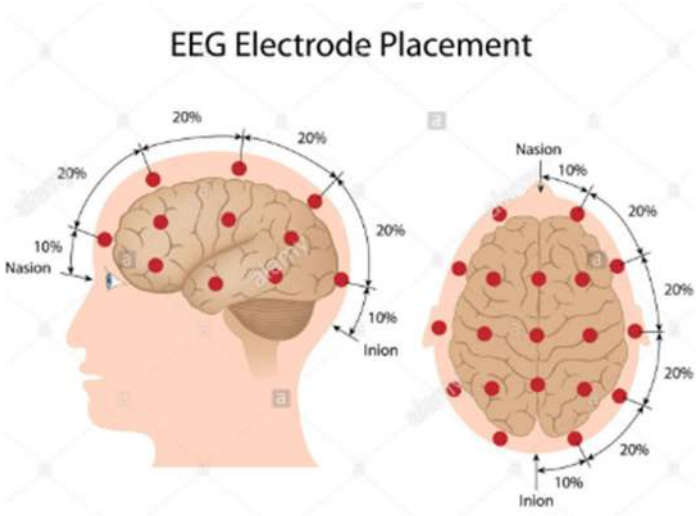

Figure 2.2: EEG electrode placement on scalp.

2.2 Field Programmable Gate Array (FPGA)

2.2.1 Introduction

The Field Programmable Gate Array, or FPGA is a programmable logic device that can have its internal configuration set by software or as it is termed, “firmware.” This enables the FPGA functionality to be updated or even totally changed as required, because the FPGA firmware is updated when it is in circuit.

2.2.2 Basic of FPGA

The great advantage of the FPGA is that the chip is completely programmable and can be re-programmed. In this way it becomes a large logic circuit that can be configured according to a design, but if changes are required it can be re-programmed with an update.

Thus, if circuit card or board is manufactured and contains an FPGA as part of the circuit, this is programmed during the manufacturing process, but can later be re-programmed to reflect any changes. Thus, it is programmable in the field, and in fact this gives rise to its name.

Although FPGAs offer many advantages, there are naturally some disadvantages. They are slower than equivalent ASICs (Application Specific Integrated Circuit) or other equivalent ICs, and additionally they are more expensive. (However, ASICs are very expensive to develop by comparison).

This means that the choice of whether to use an FPGA based design should be made early in the design cycle and will depend on such items as whether the chip will need to be re-programmed, whether equivalent functionality can be obtained elsewhere, and of course the allowable cost. Sometimes manufacturers may opt for an FPGA design for early product when bugs may still be found, and then use an ASIC when the design is fully stable. Figure 2.3 shows ALTERA DE-II board with the specifications

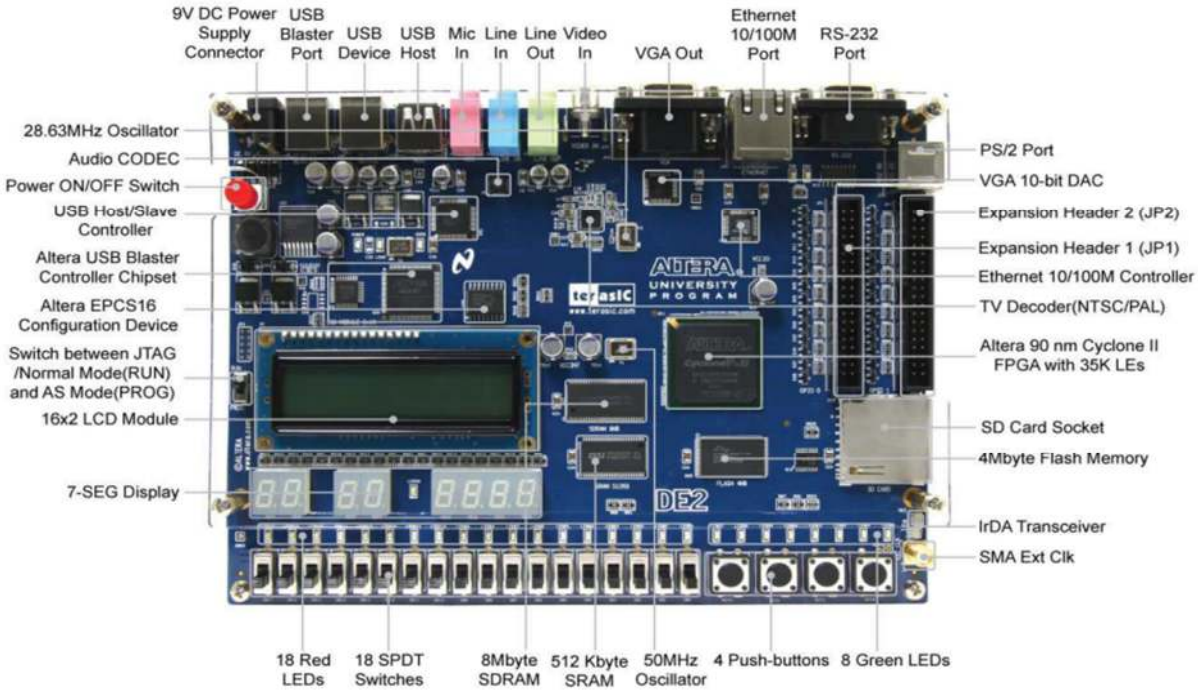

Figure 2.3: ALTERA FPGA DE2 Board

The internal resources of an FPGA chip consist of a matrix of configurable logic blocks (CLBs) surrounded by a periphery of I/O blocks. Signals are routed within the FPGA matrix by programmable interconnect switches and wire routes. The following hardware is provided on the DE2 board:

1. Altera Cyclone II FPGA device
2. USB Blaster
3. 512 KB SRAM
4. 8MB SDRAM
5. 4MB Flash memory
6. SD card
7. 4 push button switches
8. 18 toggle switches
9. 18 Red LEDs
10. 9 Green LEDs
11. Oscillator
12. VGA DAC

13. TV Decoder
14. Ethernet Port etc.

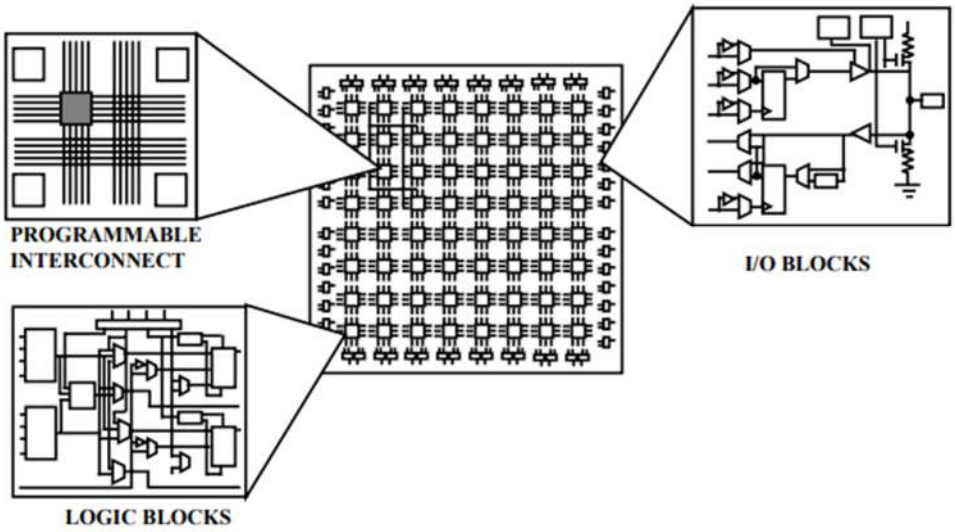

Figure 2.4: Internal resources of FPGA chip.

In an FPGA logic blocks are implemented using multiple level low fan-in gates, which gives it a more compact design compared to an implementation with two-level AND-OR logic. FPGA provides its user a way to configure: 1. the intersection between the logic blocks and 2. The function of each logic block. Logic block of an FPGA [2.7] can be configured in such a way that it can provide functionality as simple as that of transistor or as complex as that of a microprocessor. It can used to implement different combinations of combinational and sequential logic functions. Logic blocks of an FPGA can be implemented by any of the following: 1. Transistor pairs 2. Combinational gates like basic NAND gates or XOR gates 3. N-input Lookup tables 4. Multiplexers 5. Wide fan-in AND-OR structure. Routing in FPGAs consists of wire segments of varying lengths which can be interconnected via electrically programmable switches. Density of logic block used in an FPGA depends on length and number of wire segments used for routing [2.9]. Number of segments used for interconnection typically is a tradeoff between density of logic blocks used and amount of area used up for routing. Simplified version of FPGA internal architecture with routing is shown in Figure 2.5.

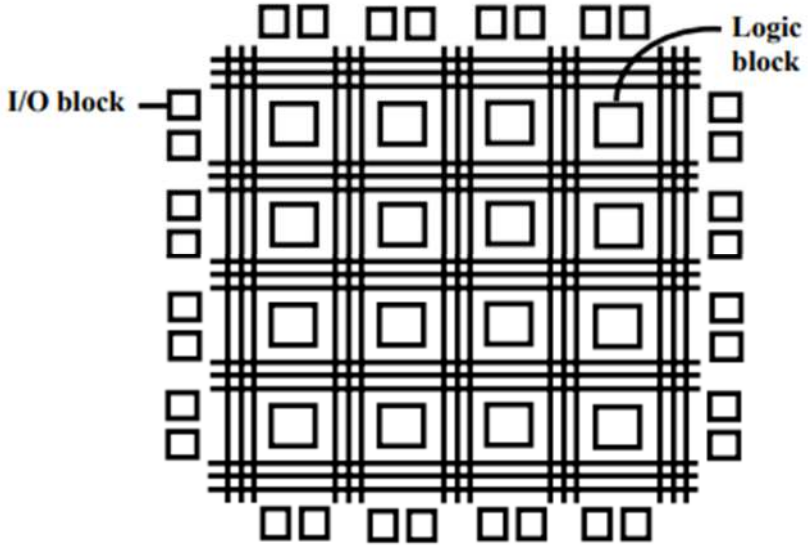

Figure 2.5: Simplified Internal Structure of FPGA.

2.2.3 Power Up the DE-II Board

The DE2 board comes with a preloaded configuration bit stream to demonstrate some features of the board. This bit stream also allows users to see quickly if the board is working properly. To power-up the board perform the following steps:

1. Connect the provided USB cable from the host computer to the USB Blaster connector on the DE2 board. For communication between the host and the DE2 board, it is necessary to install the Altera USB Blaster driver software.
2. Connect the 9V adapter to the DE2 board.
3. Connect the VGA Monitor to the VGA port on the DE2 board.
4. Connect your headset to the Line-out audio port on the DE2 board.
5. Turn the RUN/PROG switch on the left edge of the DE2 board to RUN position; the PROG position is used only for the AS Mode programming.
6. Turn the power on by pressing the ON/OFF switch on the DE2 board.

2.2.4 FPGA Device Control Panel Setup

The Control Panel Software Utility is located in the directory "DE2_control_panel" in the DE2 System CD. It's free of installation, just copy the whole folder to host computer and launch the control panel by executing the "DE2_ControlPanel.exe". Specific control circuit should be downloaded to FPGA board before the control panel can request it to perform required tasks. The program will call Quartus II tools to download the control circuit to the FPGA board through USB-Blaster [USB-0] connection [2.11]. To activate the Control Panel, perform the following steps:

1. Make sure Quartus II 12.0 or later version is installed successfully on your PC.
2. Set the RUN/PROG switch to the RUN position
3. Connect the supplied USB cable to the USB Blaster port, connect the 9V power supply, and turn the power switch ON.
4. Start the executable DE2_ControlPanel.exe on the host computer.
5. The DE2_ControlPanel.sof bit stream is loaded automatically as soon as the DE2_control_panel.exe is launched.
6. In case the connection is disconnected, click on CONNECT where the *.sof* will be re-loaded onto the board.
7. Note, the Control Panel will occupy the USB port until you close that port; you cannot use Quartus II to download a configuration file into the FPGA until the USB port is closed.
8. The Control Panel is now ready for use; experience it by setting the ON/OFF status for some LEDs and observing the result on the D1 board.

2.2.5 FPGA Design Stages

The different stages in the creation of an FPGA design are summarized as below:

1. **Design modeling:** stage is the first stage that depends on it the whole microelectronic design. The modeling design is done using Hardware Description Languages (HDL's) as VHDL (Very high-level HDL) and Verilog.
2. **Functional Verification and Simulation:** After a design has been captured as an HDL description, verification and simulation allow us to verify that the design description behaves as expected. Software tools (e.g.: ModelSim, Synopsys ...) assist a programmer to

complete this step and allow him to define simulation environments that provide the circuit description with adequate input signals.

3. **Synthesis and Optimization:** The high-level description of a circuit is mapped onto the physical resources of a reconfigurable device (e.g.: logic blocks) during the synthesis phase. Synthesis can be described as a set of transformations applied to the code in different abstraction levels.
    - **Architectural Synthesis:** It is the task of generating an architectural view for a high level model. It is also called high level synthesis because it determines the macroscopic (i.e.: block level) structure of the circuit.
    - **Logic-level Synthesis:** It is the task of generating a structural view for a high-level model. Thus, logic synthesis determines the microscopic (i.e.: gate level) structure of a circuit. Circuit optimization is often performed in conjunction with synthesis. Optimization is motivated not only by the desire of maximizing the circuit quality, but also by the fact that synthesis without optimization would yield noncompetitive circuits. Usual quality measures for circuits are area and clock frequency. Software tools are used to generate this lower level description of a circuit and to optimize the combinatorial and sequential elements of the design.
4. **Placement and Routing:** The major tasks in physical design are placement and wiring, also called routing. It consists of placing the synthesized blocks into the specific physical blocks within the hardware, and in connecting them using the reconfigurable routing. Implementation tools (e.g.: Xilinx ISE) are used to perform these tasks and generate a configuration net list that is used to configure the FPGAs. They also provide the designer with the final implementation results such as gate count, work frequency ...etc.
5. **Timing Verification:** Before the physical tests, a post place and route simulation can be performed additionally to the verifications, to verify if the implemented design behaves as 62expected. Time and area considerations may be important in order to determine if the circuit performances are sufficient.
6. **Configuration:** Configuration refers to the programming phase of an FPGA. Usually, the configuration net list is sent from the host computer to the reconfigurable device via serial

or parallel ports in order to specify its behavior. After configuration, the FPGA is assumed to act as a purpose-built circuit.

7. **Testing:** A particular feature of microelectronic circuits is the high difficulty to generate suitable testing environments. This is due to the size and complexity of present circuits. Although reconfigurable devices may be programmed in order to implement different behaviors, their physical layout is actually never changed and therefore, the testing of reconfigurable circuits has not to be repeated for every design. Only its communication with the outside world must be adapted.

2.2.6 Basic of Xilinx

Xilinx ISE (Integrated Synthesis Environment) is software tool produced by Xilinx company for synthesis and analysis of HDL (Hardware definition Language) design. Developer is also able to compile their designs, analyze timing diagram, examine RTL diagram, analyze power, voltage and current. Xilinx ISE is a design environment for FPGA product [2.10]. Verilog is used as a HDL programming language. Design hierarchy consists of modules. There is one main module for single chip design. Design constraints are specified in modules, which include pin configuration and mapping.

System level testing can be performed with ISIM or ModelSim logic simulator. Test bench program includes input signal waveforms. ModelSim or ISIM performs the following simulations [2.10].

- Logical verification to ensure that the module produce expected result.
- Behavioral verification to ensure logical and timing issues.

2.3 Summary

EEG signal which present electrical activity of brain from scalp. The advantages of FPGA technology over traditional system like much accuracy, easily reprogrammable, reduce complexity and time consumption. Although, there is some disadvantages of FPGA like need to have much knowledge about HDL language (VHDL, Verilog etc.), power consumption is more as compared to ASIC. Design and implement a Sampling Rate Conversion system using EEG on FPGA device is described in next chapter.

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CHAPTER III

Sampling Rate Conversion System Method-I

Chapter Outlines

- Introduction
- Materials and Methods
- Processing Algorithm for Sampling Rate Conversion System
- Experimental Result Analysis
- Summary
- References

CHAPTER III

Sampling Rate Conversion System Method-I

3.1 Introduction

The EEG signal contains noises and artifacts during the recording of the EEG signal. The noise from the main source should be eliminated to increase accuracy of biosignal processing in bio-chip system. However, there is no need to consider high speed processing and has no effect on the analysis data with a minimum delay of the data measurement procedure [3.2-3.3]. For real time EEG signal analysis, it is argued that software processing is not sufficient and hardware processing needs to be involved. Hardware processing is fast and can provide portability due to its small size. The proposed system works with sampling rate conversion for high speed data and lower time resolution. The main concept of this design is used to change the sampling rate of a signal. The process of decreasing the sampling rate is called *decimation*, and the process of increasing the sampling rate is called *interpolation*.

3.2 Materials and Methods

Materials and Methods which are used are describes below: -

3.2.1 Data Analysis

The raw EEG data of signals are collected from BME signal processing lab from department of Biomedical Engineering. The data (EEG) is taken on Biopac system [3.1] and has been collected from this software for further processing. EEG data was taken from 3 students. This biopac device contains three leads.

I. Red Lead
II. White Lead

III. Black Lead

Make sure that the electrode has appropriate contact with the skin and collect EEG signal data from the scalp. For appropriate contact electrolyte gel is used. Red lead is placed at the frontal right of head on the electrode, white lead is at the left frontal on the electrode and black lead is placed behind the ear on the electrode. Electrode should contain appropriate amount of paste for solid electrical contact. Output EEG data which come from scalp are plotted on the software within the computer. After that the decimal data are collected from the plotted image.

The condition for recording EEG signal was solving puzzle. This raw data has included some artifacts into the EEG signals.

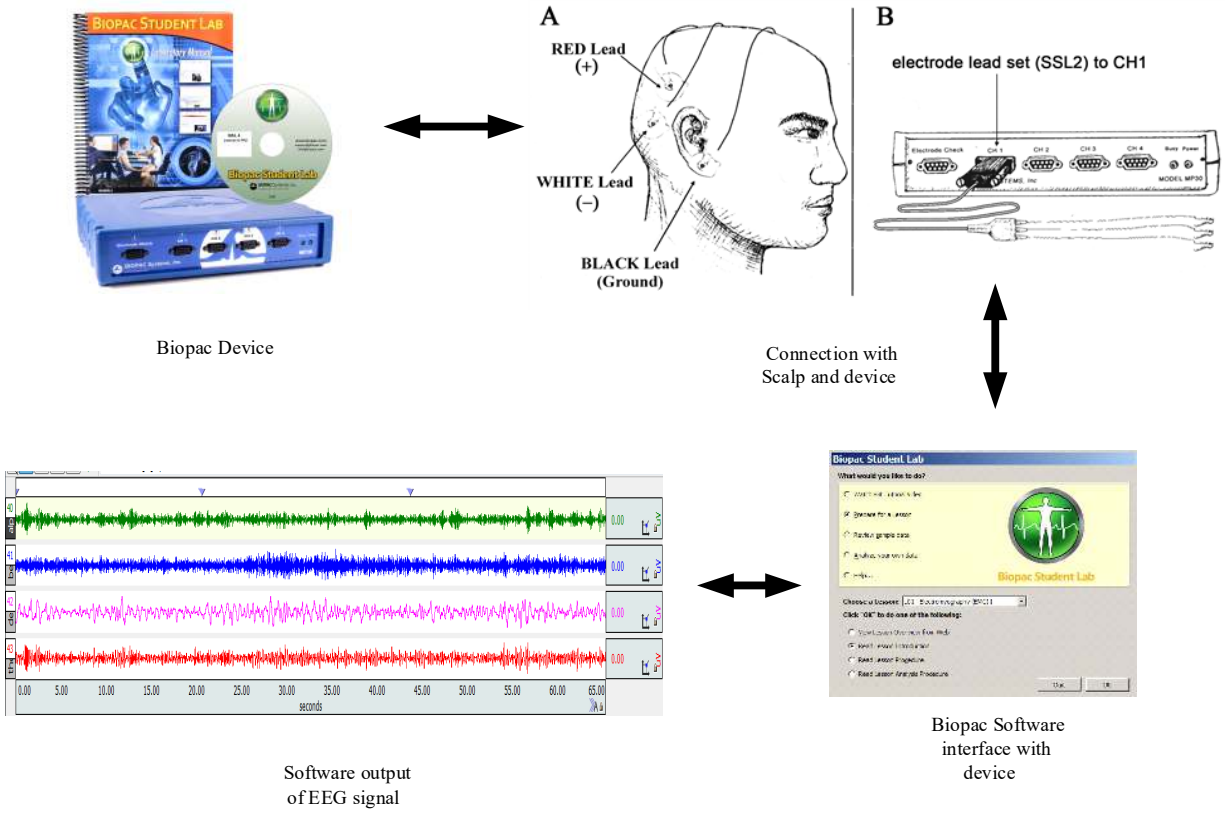


Figure 3.1: Data acquisition flow chart.

Figure 3.2 shows the recorded view of the EEG signal. Which display on Biopac interface software installed within the computer.

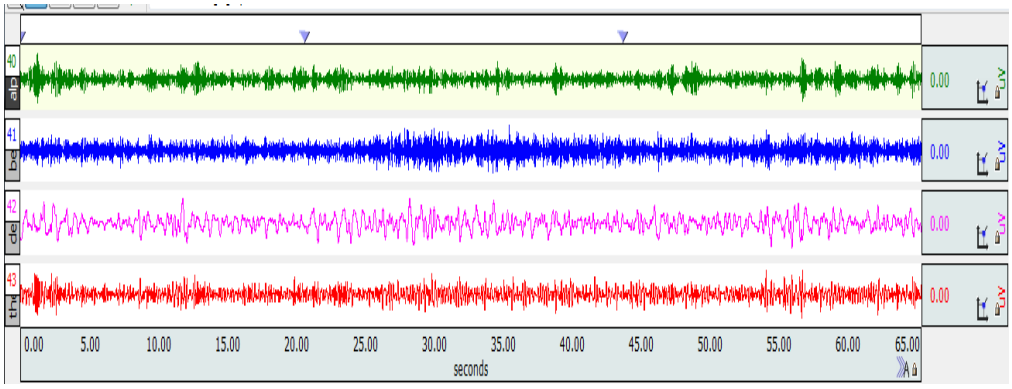


Figure: 3.2: Recorded EEG signal.

3.2.2 Proposed Methodology 1 for Sampling Rate Conversion System

The proposed system has been considered on sampling rate conversion (SRC) for biomedical signal processing applications. The way to SRC is to connect an ADC in series with a DAC to first convert the continuous signal $x(t)$ to sequence $x[n]$ and then back into the time domain at the new sampling rate $f_{s,new}$. There are three kinds of SRC: decreasing sampling rate (called *Decimation* where$f_{s,new} < f_{s,old}$), increasing it (called *Interpolation* where $f_{s,new} > f_{s,old}$), synchronizing two signals with the same sampling frequency ($f_{s,new} = f_{s,old}$). Here, we have considered two different cases where the sampling rate of signal $x[n]$ is increased by sampling rate L, then filtered using digital filter and after that decreasing the sampling rate by sampling rate M, where for case (i) $L = M$; and case (ii) $L \neq M$.

A simple block diagram representation of the proposed sampling rate conversion system is given in Figure 3.3 where h(n) is an anti-aliasing digital filter. This proposed system considers direct form of digital filter implementation, the output of the filter, $y(n)$ and the input $x(n)$, the filter equation is as follows,

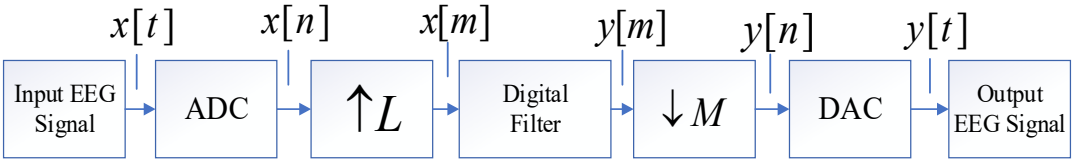


Figure 3.3: Block diagram of sampling rate conversion system.

$$y(n) = -\frac{3}{35}x(n) + \frac{12}{35}x(n-1) + \frac{17}{35}x(n-2) + \frac{12}{35}x(n-3) - \frac{3}{35}x(n-4) \qquad (3.1)$$

Apply z-transform on both side of the equation (3.1) we get:-

$$Y(z) = \left(\frac{-3}{35}x(z) + \frac{12}{35}x(z)z^{-1} + \frac{17}{35}x(z)z^{-2} + \frac{12}{35}x(z)z^{-3} - \frac{3}{35}x(z)z^{-4}\right)$$

$$Y(z) = \left(\frac{-3}{35} + \frac{12}{35}z^{-1} + \frac{17}{35}z^{-2} + \frac{12}{35}z^{-3} - \frac{3}{35}z^{-4}\right)X(z)$$

$$\frac{\boldsymbol{Y(z)}}{\boldsymbol{X(z)}} = \boldsymbol{H(z)} = \left(\frac{\boldsymbol{-3}}{\boldsymbol{35}} + \frac{\boldsymbol{12}}{\boldsymbol{35}}\boldsymbol{z^{-1}} + \frac{\boldsymbol{17}}{\boldsymbol{35}}\boldsymbol{z^{-2}} + \frac{\boldsymbol{12}}{\boldsymbol{35}}\boldsymbol{z^{-3}} - \frac{\boldsymbol{3}}{\boldsymbol{35}}\boldsymbol{z^{-4}}\right) \quad (3.2)$$

Then substitute the z:

$$H(e^{j\omega}) = \frac{-3}{35} + \frac{12}{35}e^{-j\omega} + \frac{17}{35}e^{-j2\omega} + \frac{12}{35}e^{-j3\omega} - \frac{3}{35}e^{-j4\omega} \quad (3.3)$$

$$H\left(e^{j\omega}\right) = \frac{-3}{35} + \left\{\frac{12}{35}(\cos\omega - j\sin\omega)\right\} + \left\{\frac{17}{35}(\cos 2\omega - j\sin 2\omega)\right\}$$
$$+ \left\{\frac{12}{35}(\cos 3\omega - j\sin 3\omega)\right\} - \left\{\frac{3}{35}(\cos 4\omega - j\sin 4\omega)\right\}$$
$$= \frac{-3}{35} + \frac{12}{35}\cos\omega - j\frac{12}{35}\sin\omega + \frac{17}{35}\cos 2\omega - j\frac{17}{35}\sin 2\omega$$
$$+ \frac{12}{35}\cos 3\omega - j\frac{12}{35}\sin 3\omega - \frac{3}{35}\cos 4\omega + j\frac{3}{35}\sin 4\omega$$
$$= \frac{-3}{35} + \left(\frac{12}{35}\cos\omega + \frac{17}{35}\cos 2\omega + \frac{12}{35}\cos 3\omega - \frac{3}{35}\cos 4\omega\right)$$
$$-j\left(\frac{12}{35}\sin\omega + \frac{17}{35}\sin 2\omega + \frac{12}{35}\sin 3\omega - \frac{3}{35}\sin 4\omega\right) \quad (3.4)$$

Magnitude response of the first method equation is as follows:-

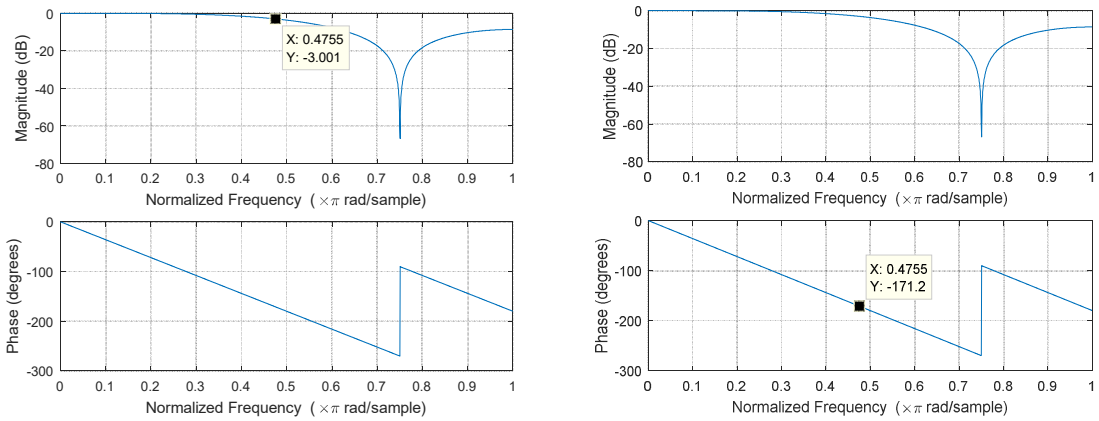
$$\left|H(e^{jw})\right| = \sqrt{\begin{array}{l}\left(\frac{-3}{35} + \frac{12}{35}\cos\omega + \frac{17}{35}\cos 2\omega + \frac{12}{35}\cos 3\omega - \frac{3}{35}\cos 4\omega\right)^2 \\ + \left(\frac{12}{35}\sin\omega + \frac{17}{35}\sin 2\omega + \frac{12}{35}\sin 3\omega - \frac{3}{35}\sin 4\omega\right)^2\end{array}} \quad (3.5)$$

Phase response of the filter is as follows: -

$$\varphi(\omega) = tan^{-1}\frac{-\left(\frac{12}{35}\sin\omega + \frac{17}{35}\sin 2\omega + \frac{12}{35}\sin 3\omega - \frac{3}{35}\sin 4\omega\right)}{\left(\frac{-3}{35} + \frac{12}{35}\cos\omega + \frac{17}{35}\cos 2\omega + \frac{12}{35}\cos 3\omega - \frac{3}{35}\cos 4\omega\right)} \quad (3.6)$$

$H(z)$ is the transfer function, where $X(z)$ and $Y(z)$ are the z-transforms of $x(n)$ and $y(n)$ respectively. The frequency response of a system is obtained by evaluating its transfer function at various point on the unit circle in the z-plane, that is by letting z $= \exp(j\omega)$ and evaluating $H(z)$ for various values of the frequency variable ω. Magnitude transfer function of a system for a

particular value of z is given by the product of the distances from the corresponding point in the z-plane to all the zeroes of the system's transfer function, divided by the product of the distances to its poles. The phase response is given by the sum of the angles of the vectors joining the point to all the zeroes, minus the sum of the angles to the poles.



(a) (b)

Figure 3.4: Frequency and phase response of the proposed system.

Figure 3.4 (a) & (b) shows the frequency response and phase response of the filter. From the plotting of Figure of 3.4 (a), It's frequency response is looks like a parabolic filter. Phase of this filter is linear. When $\omega = 0$, value of $\left|H(e^{jw})\right| = 1$ and $\left|H(e^{jw})\right| = 0.707 = 3dB$ (from Figure 3.4 (a)) when $\omega = 0.4755\pi$ (from the Figure of 3.4).

So,

$$\omega = 0.4755\pi$$

$$2\pi f = 0.4755\pi$$

$f = 0.24$Hz which is the digital frequency.

Analog frequency can drive from the value of digital frequency f

$$\frac{f_c}{f_s} = f$$

$$f_c = f f_s$$

Considering the sampling frequency is 1000 Hz, then the cutoff frequency would be,

$$= 0.24 * 1000$$

$$= 240\ Hz$$

Let $z = e^{sT}$, where T=sampling period, since $s = \sigma + j\omega$, we have

$$z = e^{\sigma T} e^{j\omega T}$$

If $\sigma = 0$, then $|z| = 1$ and $z = e^{j\omega T} = \cos \omega T + j \sin \omega T$, i.e. the equation of a circle of unit radius in the z-plane. Phase response equation is

$$Arg\left[H\left(e^{j\omega}\right)\right] = atan\left(\frac{Im[H\left(e^{j\omega}\right)]}{Re[H(e^{j\omega})]}\right)$$

Where Arg[.] denotes the principal value of the phase, and where $\omega = 2\pi fT$, for T the sample period. The arctangent function atan(x) is an anti-symmetrical function (of an anti-symmetrical variable x). The imaginary part of $H\left(e^{j\omega}\right)$is an anti-symmetrical function of frequency, while its real part is a symmetrical function. The variable $Im\left[H\left(e^{j\omega}\right)\right]/Re[H\left(e^{j\omega}\right)]$ is therefore antisymmetrical, hence phase response is anti-symmetrical versus ω.

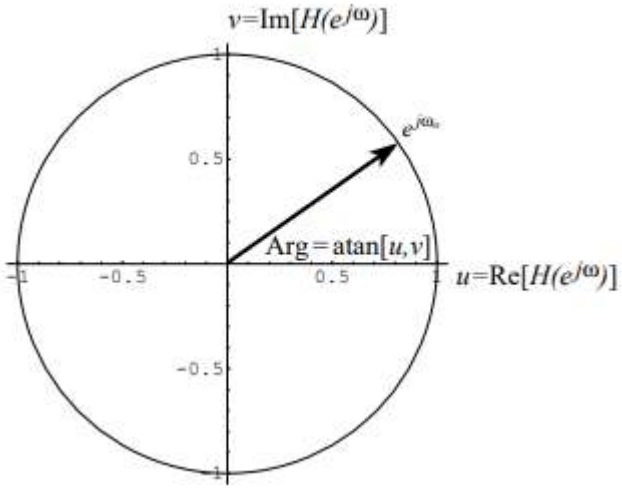


Figure 3.5: Pole zero analysis of method I.

The normalized radian frequency ω = 0 corresponds to the coordinate (1,0), while ω = ± π corresponds to (-1, 0). By tracing $H\left(e^{j\omega}\right)$ with ω, while measuring the angle of the vector from the origin to the corresponding point on the contour, we see that ArgII[.] is clearly wrong in this case $H\left(e^{j\omega}\right) = e^{j\omega}$ and, by induction, wrong in general.

Phase response of the equation (3.1)

$$ArcTan\left[-\frac{3}{35}+\frac{12}{35}\cos[\omega]+\frac{17}{35}\cos[2\omega]\right.$$
$$+\frac{12}{35}\cos[3\omega]-\frac{3}{35}\cos[4\omega],-\frac{12}{35}\sin[\omega]-\frac{17}{35}\sin[2\omega]$$
$$\left.-\frac{12}{35}\sin[3\omega]+\frac{3}{35}\sin[4\omega]\right]/\pi$$

Figure 3.6 shows the pole-zero diagram of the filter of method I. Pole zero diagram can be obtained from the frequency response of the filter. Small circle denotes zero and small cross sign denotes pole. A filter will be stable when it's all poles in the z-plane inside the unit circle. FIR filters are always stable because they have only one poles at the center position of the unit circle. This filter is a five-point filter so there is four number of zeroes in the diagram.

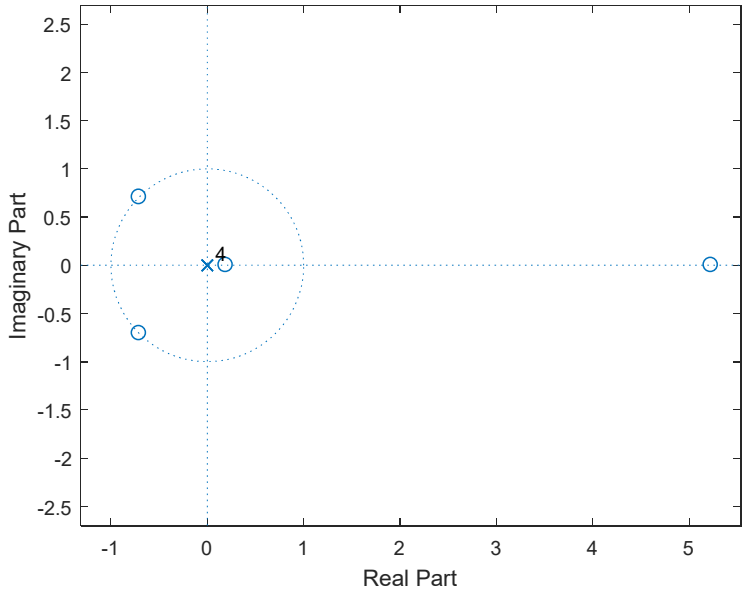


Figure 3.6: Pole-zero diagram of the method I.

The proposed SRC system have assigned some paprameters on input-output relationship for each block and its signal flow graph is shown in Figure 3.7. For every input sample, $x(n)$ fed into the interpolator, after interpolation there are $L-1$ zero valued sample within sample $x(n)$. These are then filtered using digital filter to yield $y(m)$. Thus for each input samples for $x(n)$, L samples of $y(m)$. Effectively, the input sampling frequeny is increased from f_s to Lf_s by the interpolator. One implication of inserting $L-1$ zeroes after each sample is that the energy of each input sample

is spread across L output samples.Thus the interpolator has a gain of $1/L$. After interpolation , each output samples should be multiplied by L to restore its proper level.

Each input sample fed in, three samples are computed. The non zero samples (that is the actual samples of $x(n)$ in the delay line are seperated by $L-1$ zeroes). Clearly, multiplication operations by the zero valued samples are unnecessary.

The interpolation equation is

$$x(n) = x\left(\frac{n}{L}\right) \tag{3.7}$$

Now equation (3.1) can be re written for up sampling as,

$$y_L\left(\frac{m}{L}\right) = y_L(m) = -\frac{3}{35}x\left(\frac{n}{L}\right) + \frac{12}{35}x\left(\frac{n}{L}-1\right) + \frac{17}{35}x\left(\frac{n}{L}-2\right) + \frac{12}{35}x\left(\frac{n}{L}-3\right) - \frac{3}{35}x(\frac{n}{L}-4) \tag{3.8}$$

Decimation equation is

$$x(n) = x(nM) \tag{3.9}$$

Now the down sampling equation is,

$$y_M(m) = \mathrm{y_L}(mM) = -\frac{3}{35}x\left(\frac{nM}{L}\right) + \frac{12}{35}x\left(\frac{nM}{L}-1\right) + \frac{17}{35}x\left(\frac{nM}{L}-2\right) + \frac{12}{35}x\left(\frac{nM}{L}-3\right) - \frac{3}{35}x(\frac{nM}{L}-4) \tag{3.10}$$

The input $y_L(\mathrm{m})$ is fed into the delay line one sample at a time. For every M samples of $y_L(\mathrm{m})$ applied to the delay line one output sample $y_M[n]$. This involves keeping the first sample of $y_L(\mathrm{m})$, discarding the next M-1 samples, keeping the next sample, and discarding the next M-1 samples, and so on. Since for each sample that is kept, the next M-1 samples of $y_L(\mathrm{m})$ are discarded, it is necessary to perform by the equation (3.9) for those samples of $y_L(\mathrm{m})$ that are discarded.

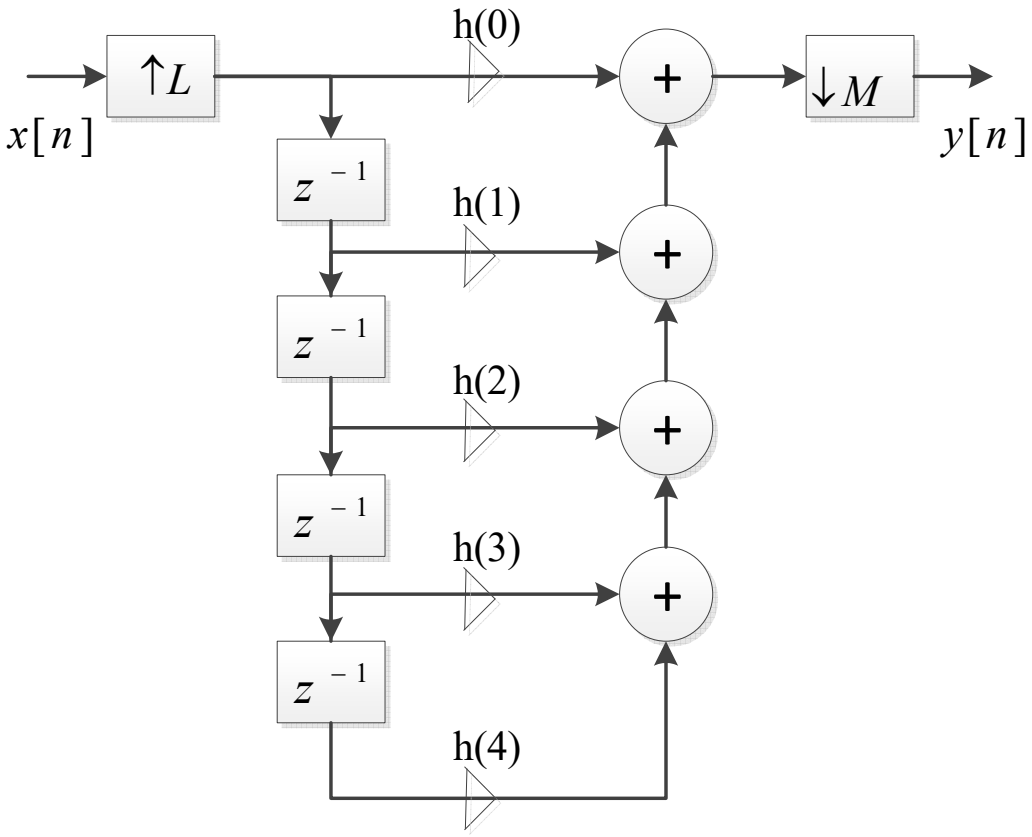


Figure 3.7: The signal flow graph of proposed sampling rate conversion system method I.

3.2.3 Flow Charts of Sampling Rate Conversion System:

Figure 3.7 shows a flowchart for the proposed sampling rate conversion system operations for case I with interface ALTERA Cyclone DE II Device using processors EP2C35F672C6. For up sampling operations the input EEG signal is converted to binary by ADC and up sampled or interpolator by L which is also in binary. In this implementation , only the non zero valued samples are fetched and used in the computation of the output samples . We see that, at each sampling instant into digital filter, we must first shift the data by one place, read and save the latest input sample, x[n] and compute the current output sample using the equation (3.7) We also used the equation (3.9) for the operation of down sampling by M and use DAC to get output $y(t)$. For the case II we just use $L = 3$ and $M = 2$ into the flow chart.

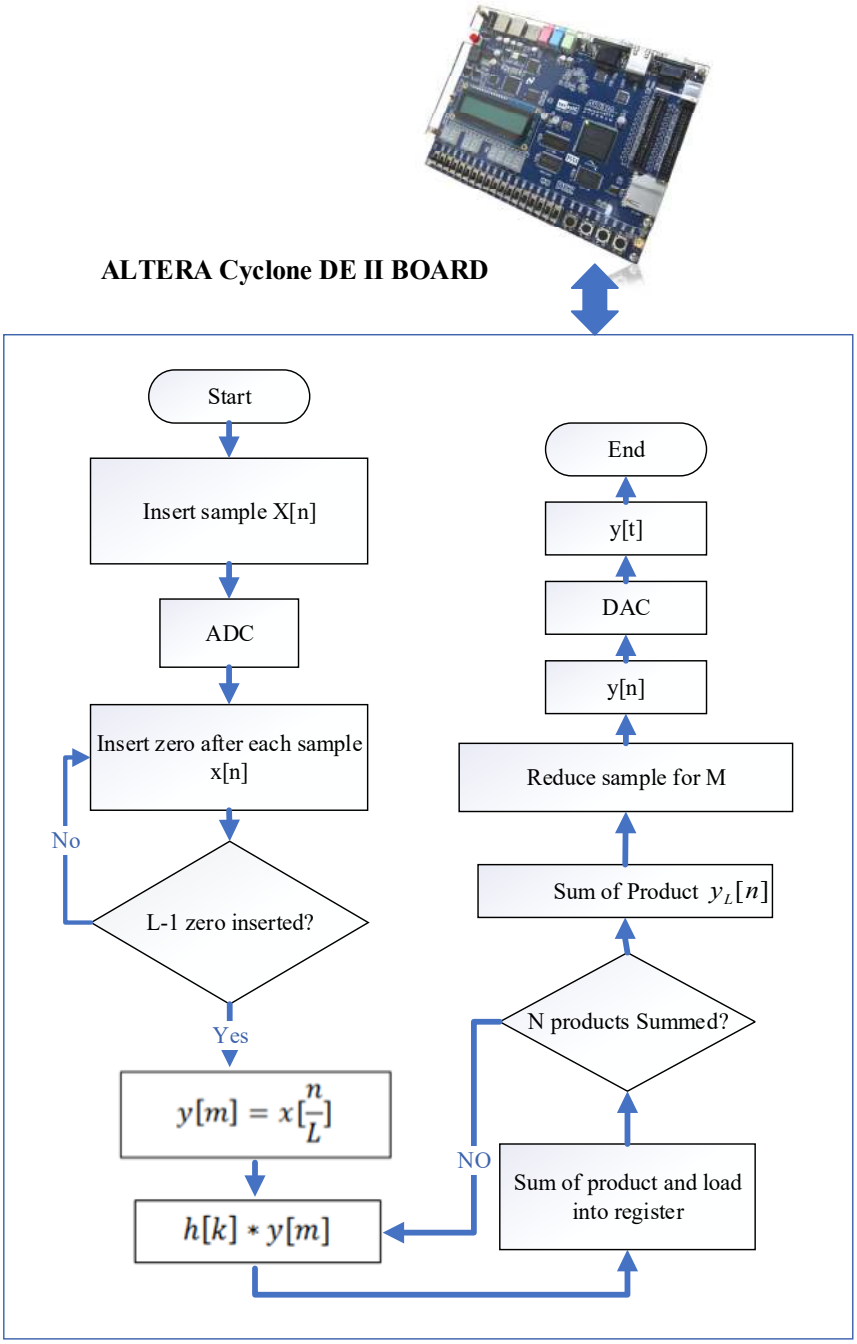


Figure 3.8: A simplified flowchart of proposed SRC system with interface ALTERA Cyclone DE II Board.

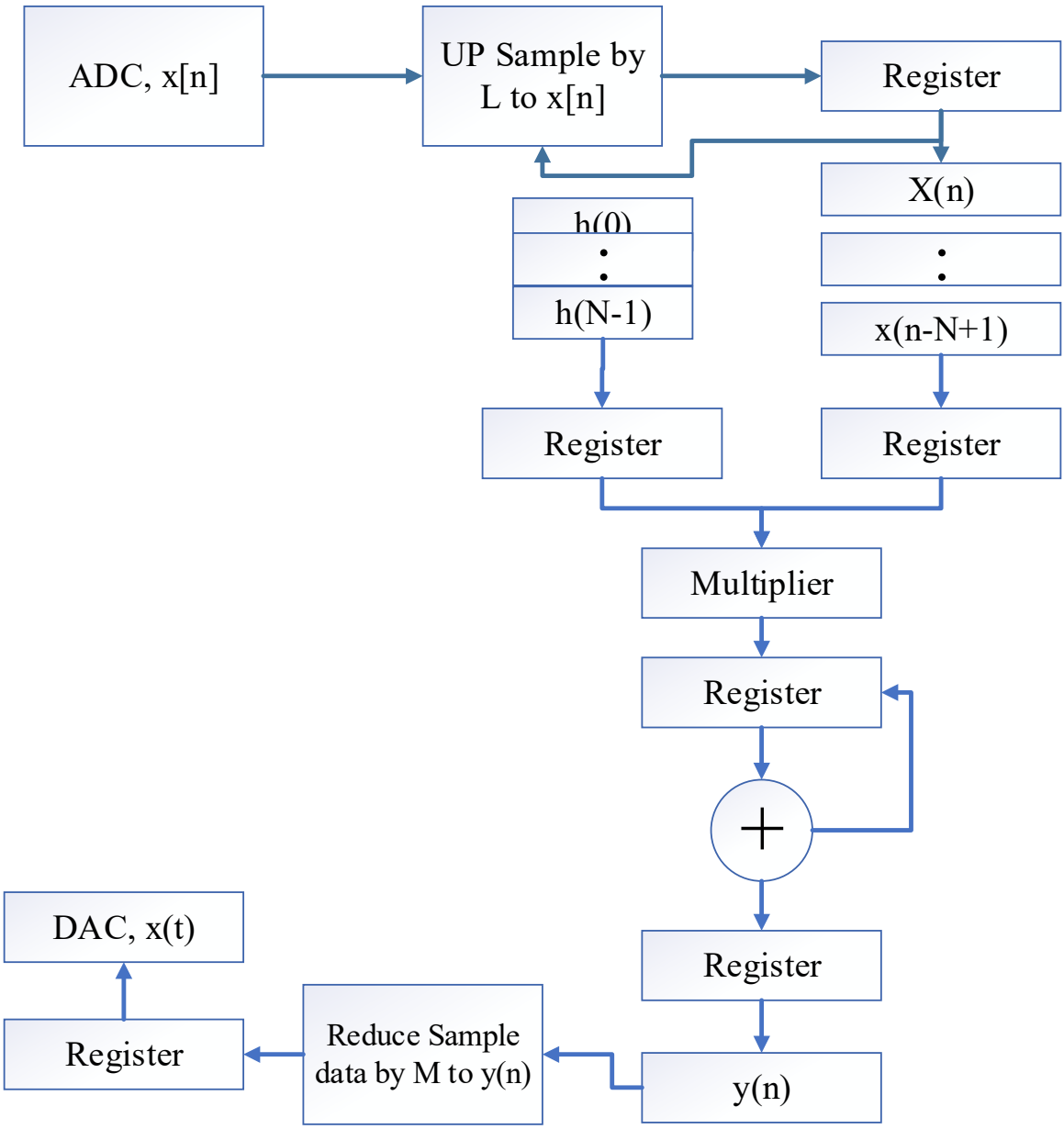


Figure 3.9: Pipeline MAC configuration of proposed sampling rate conversion system.

Figure 3.9 shows pipelined MAC configuration of proposed system for executing the sampling rate conversion system using equation (3.7) and (3.9)

a. The arithmetic operation of the proposed sampling rate conversion system can be expressed into three distinct steps**:** memory read, multiply and accumulates**.**
b. Adds the previous product to the accumulator**-** initially, the product is zero**.**
c. EEG signal decimal data are converted by ADC and stored $x[n]$ data into auxiliary register**.**

d. Increase the discrete samples data of $x[n]$ by L **(**Interpolator**)** and stored $L * x[n]$ data into auxiliary register**.**
e. The coefficients a_k by the data memory $x[n]$ accessed sequentially and applied to the multiplier**.** The products are summed in the accumulator and store into auxiliary register **(**AR**).** Initially AR point's $x[n]$ and then successively, points $x[n-N+1]$ decrement the address by 1 where we have used D flip flop for shift register operation for unit delay of samples**.**
f. Store sampled filtered output $y_L(n)$ into register**.**
g. Decrease the sampling rate of $y_L(n)$ M $(y_L(n)/M)$ and store within the register**.**
h. Finally, we get discrete output $y(n)$ and store it into the register**.**
i. Then apply DAC of $y[n]$ and get the values of $y(t)$**.**

3.3 Processing Algorithm for Sampling Rate Conversion System

For real time digital filtering, the data x[n] and coefficients h[n] are stored in memory, conceptually. At first the data x[n] is increasing the sample by the factor L. If we consider EEG signal elements as illustrate follows are

$$x[n] = [1, 2, 3, 4, 5, 6, 7, 8, 9, \dots.]$$

Up-sample by $L = 2$ of $x[n]$, it will happen as

$$x[n] = [1, 0, 2, 0, 3, 0, 4, 0, 5, 0, 6, 0, 7, 0, 8, 0, 9, \dots.]$$

These sequences are applied to digital filter. To appreciate how the digital filter works, consider the simple case of $N = 5$, with the following equation by :

$$y(n) = \frac{-3}{35}x(n) + \frac{12}{35}x(n-1) + \frac{17}{35}x(n-2) + \frac{12}{35}x(n-3) + \frac{-3}{35}x(n-4)$$

where $x(n)$ represents the latest input sample, $x(n-1)$ the last sample, and $x(n-2)$ the sample before last.

Suppose the four-coefficients digital filter is fed from an ADC. The first thing to do is to allocate two sets of contigious memory locations (in RAM), one for storing the input data ($x(n),\ x(n-1),\ x(n-2),\ x(n-3),\ x(n-4)$) and the other for the filter coefficients ($h(0),\ h(1),\ h(2),\ h(4)$) as depicted below:

Data in RAM	Coeeficients in Memory
$\frac{-3}{35}$	$h(0)$
$\frac{12}{35}$	$h(1)$
$\frac{17}{35}$	$h(2)$
$\frac{12}{35}$	$h(3)$
$\frac{-3}{35}$	$h(4)$

At initialization, the RAM locations where the data samples are to be stored are set to zero since always start with no data . The following operations are then performed:

- *First sampling instant:* To read data sample from the ADC and then up-sampled by L into x[n], shift data RAM one place (to make for the new data), to save the new input sample , compute output sample and then to send the computed output sample and the DAC before down-sample by M.

Data in RAM	Coefficients in Memory	
$x(1)$	$\frac{-3}{35}$	$y(1) = \frac{-3}{35}x(1) + \frac{12}{35}x(0) + \frac{17}{35}x(-1) + \frac{12}{35}x(-2) + \frac{-3}{35}x(-3)$
$x(0) = 0$	$\frac{12}{35}$	
$x(-1) = 0$	$\frac{17}{35}$	
$x(-2) = 0$	$\frac{12}{35}$	
$x(-3) = 0$	$\frac{-3}{35}$	

- *Second sampling instant:* Repeat the above operations and work out samples and send to the DAC.

Data in RAM	Coefficients in Memory	
$x(2)$	$\frac{-3}{35}$	$y(2) = \frac{-3}{35}x(2) + \frac{12}{35}x(1) + \frac{17}{35}x(0) + \frac{12}{35}x(-1) + \frac{-3}{35}x(-2)$
$x(1)$	$\frac{12}{35}$	
$x(0) = 0$	$\frac{17}{35}$	
$x(-1) = 0$	$\frac{12}{35}$	
$x(-2) = 0$	$\frac{-3}{35}$	

- *nth sampling instant:* Repeat the above operations and work out samples and send to the DAC.

Data in RAM	Coefficients in Memory	
$x(5)$	$\frac{-3}{35}$	$y(n) = \frac{-3}{35}x(n) + \frac{12}{35}x(n-1) + \frac{17}{35}x(n-2) + \frac{12}{35}x(n-3) + \frac{-3}{35}x(n-4)$
$x(4)$	$\frac{12}{35}$	
$x(3)$	$\frac{17}{35}$	
$x(2)$	$\frac{12}{35}$	
$x(1)$	$\frac{-3}{35}$	

3.3.1 Up sampling

The Figure 3.10 illustrates the flowchart of the up-sampling process was used in both cases. We have used the raw EEG data that was described in chapter II. The simulation program has considered few parameters to execute the total up-sampling procedures. Data are stored in 8-bit registers. The main motto in this operation is to increase the sampling rate of signal. For example,

if the sequences of the samples of EEG signal are like $(1, 2, 3, 4, 5, 6 \ldots \ldots)$ then the resulting sequences of samples are like $(1, 0, 2, 0, 3, 0, 4, 0, 5, 0, 6, 0 \ldots \ldots)$ for $L = 2$. The advantage of up-sampling is, it can increase the sampling rate of the signal as we wish for detailed processing of the EEG signal. So, by increasing the value of L as we require, we can scrutinize the signal more precisely for better analysis.

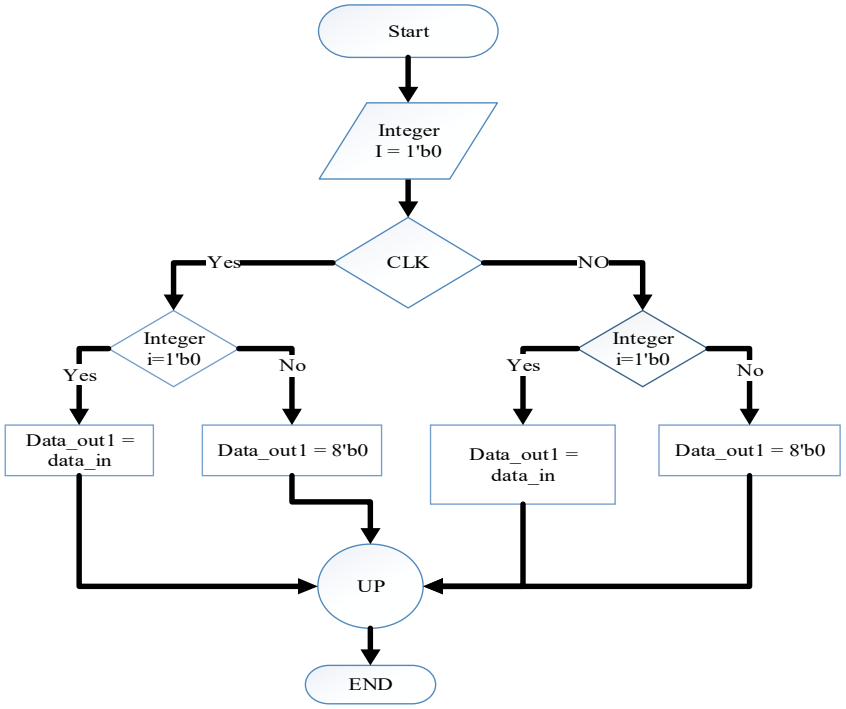


Figure 3.10: Flowchart of the up-sampling process using Xilinx.

3.3.2 Digital Filter Design Structure in FPGA

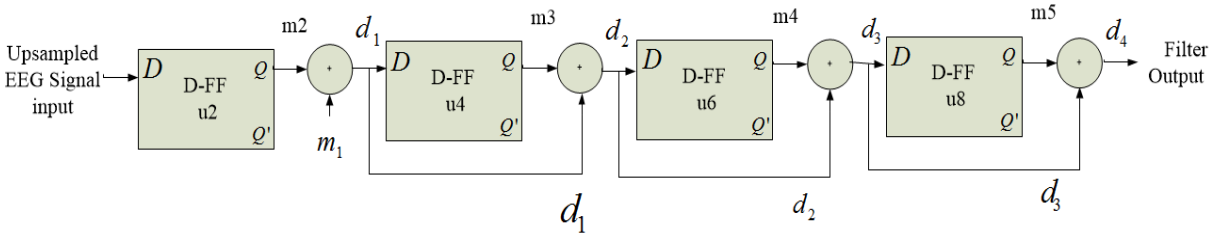


Figure 3.11: Basic diagram of designed digital filter operations.

Figure 3.11 illustrates the basic block diagram of the digital filter. In this block, we have used four D flip flops for 4-unit delay operations. At first, the input is used up-sampled values $x[m]$ which was stored into register. These up-sampled values are processed with following procedures as described below. The EEG data signals which are up sampled are the direct input considered as m_1.

- The 2nd D flip flops input is d_1 = {m_2 (output of the 1st D flip flop) + m_1}
  Output = m3
- The 3rd D flip flops input is d_2 = {$d_1(m_1 + m_2)$ + m_3 (output of the2nd D flip flop)}
  Output = m_4
- The 4th D flip flops input is d_3 = {m_4 (output of the 3rd D flip flop) + d_2}
  Output = m_5
- The final output = d_4 ={m_5 (output of the 4th D flip flop) + d_3}

3.3.3 Down sampling:

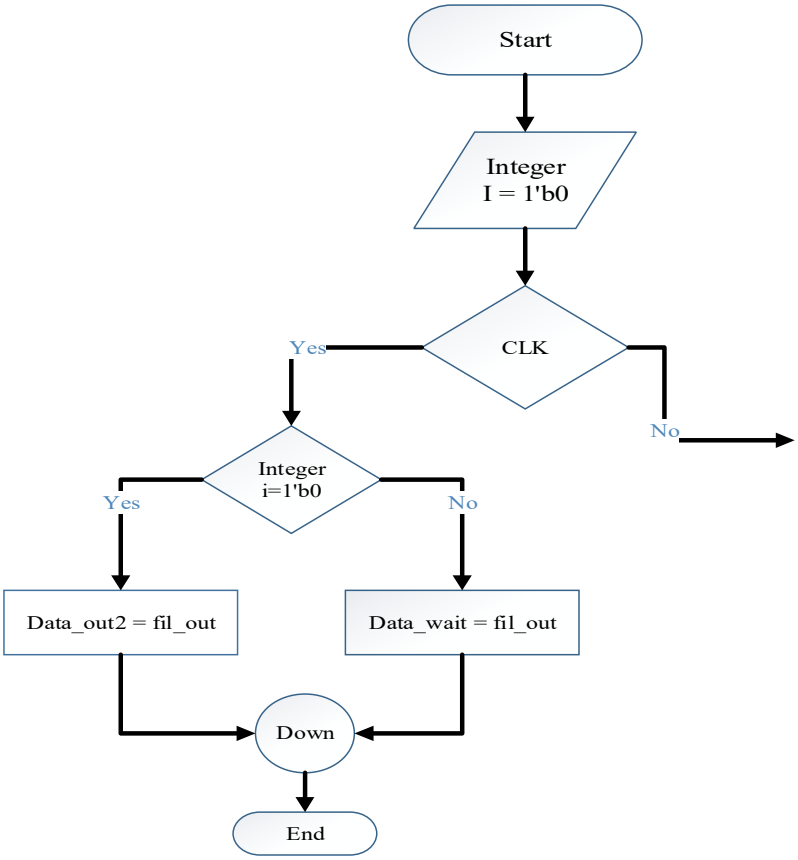


Figure 3.12: Flowchart of the down-sampling process using Xilinx.

Figure 3.12 shows the flowchart of the down-sampling process. Like up-sampling, it has considered some parameters for performing down-sampling operation. These data are stored in 8-bit registers. The main aim is to decrease the sampling rate of the filtered signal. For example, if

we consider the input sequence of EEG signal like $(1, 2, 3, 4, 5, 6, 7, 8 \dots \dots)$ then the down sampled value is like $(1, 3, 5, 7 \dots \dots)$ for $M = 2$. By increasing the value of M, we can decrease the down-sampling rate for reducing samples according to the requirements. So, down-sampling is the counter action of up-sampling.

3.4 Experimental Result Analysis

The methodology described in this chapter which are implemented by The ALTRA DE2 Quartus II software which supports devices family Cyclone II FPGA Kit and also the Xilinx ISE 4.7 design suite. By implementing the processes, the main working procedures are: find out the flowchart simulation, analyze the RTL block diagram, timing diagram and find out its operating parameters. Finally, the results will show.

3.4.1 RTL Diagram of Sampling Rate Conversion System

In the early stage, registers have been used to perform up-sampling operations. For every clock pulse, an input data has been taken and the input is stored in an intermediate register. Next, Data containing zero value is inserted into register within the next clock pulse. Furthermore, for digital filter operation, we have used D flip-flops as memory element and it has connected with four D Flip-flops in series in order to obtain the Shift Register operation where input clock and reset value controls the D flip-flops. Finally, The Down-sampling operation is performed by again using registers. Within the RTL block, multiplexers (MUX 2:1) and Lookup tables(4-LUT) have been used to generate logic operations. Here, registers have been used to store each and every data. Again, multipliers, 8-bit adders, latches are used in the RTL diagram as shown in Table-3.1 below. Next, Table 3.2 shows that the core temperature was $27.2^{\circ}C$ during the simulation process. Table 3.2 also shows the voltage supply (V_{cc}), total current and total power needed for the proposed system design.

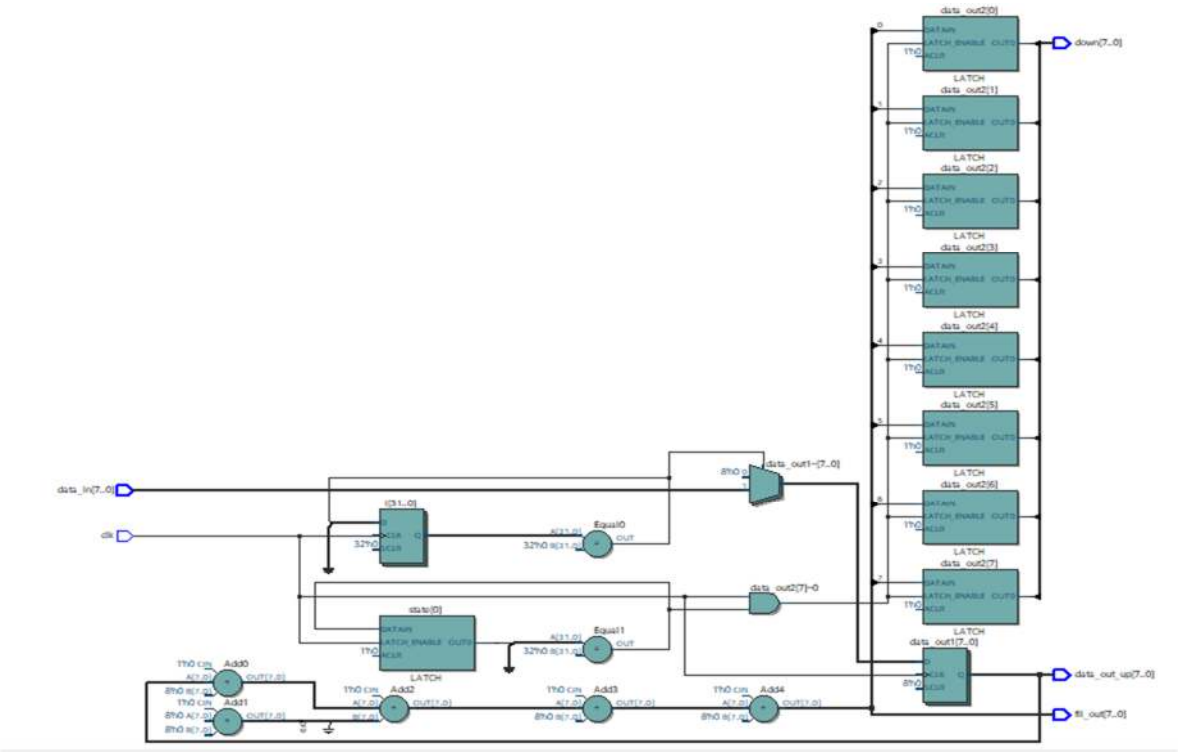


Figure 3.13: RTL diagram for Sampling Rate Conversion System.

Table 3.1: HDL Synthesis Report (Macro Statistics)

Multipliers	3
8x2-bit multiplier 8x3-bit multiplier	2 1
Adders/Sub-tractors (8-bit adder)	4
Registers (D Flip-Flops)	72
Latches (8-bit latch)	1
IOs	33
Total no. of paths	32

Table 3.2: Power analyzer report of Sampling Rate Conversion System.

Core temp.	$27.2^{\circ}C$
Voltage supply(v_{cc})	2.4V
Total Current (A)	0.016A
Total Power(W)	0.08W

Table 3.3: Setup Time

Data Port	Clock Port	Rise	Fall	Clock edge	Clock Reference
KEY[*]	KEY[0]	2.876	2.876	Rise	KEY[0]
KEY[1]	KEY[0]	2.876	2.876	Rise	KEY[0]
SW[*]	KEY[0]	0.986	0.986	Rise	KEY[0]
SW[0]	KEY[0]	0.445	0.445	Rise	KEY[0]
SW[1]	KEY[0]	0.381	0.381	Rise	KEY[0]
SW[2]	KEY[0]	0.226	0.226	Rise	KEY[0]
SW[3]	KEY[0]	0.312	0.312	Rise	KEY[0]
SW[4]	KEY[0]	0.140	0.140	Rise	KEY[0]

3.4.2 Timing Diagram:

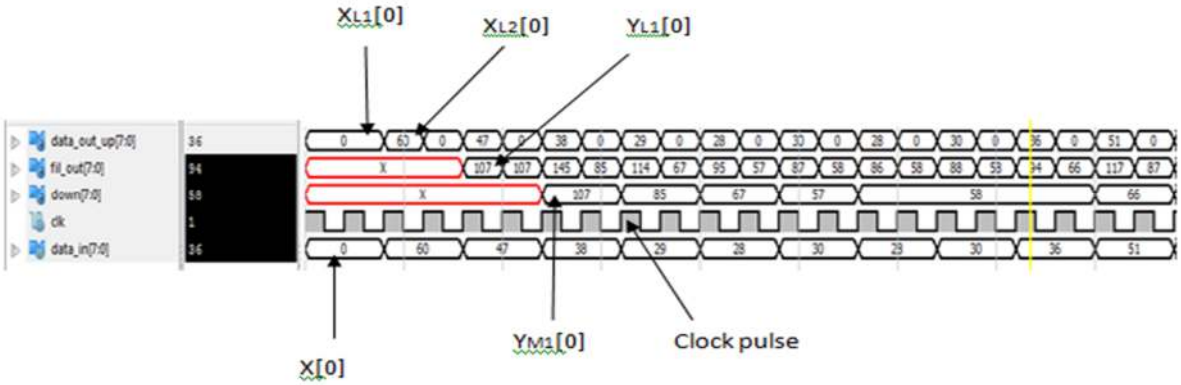


Figure 3.14: Timing Diagram of $L = 2$ and $M = 2$.

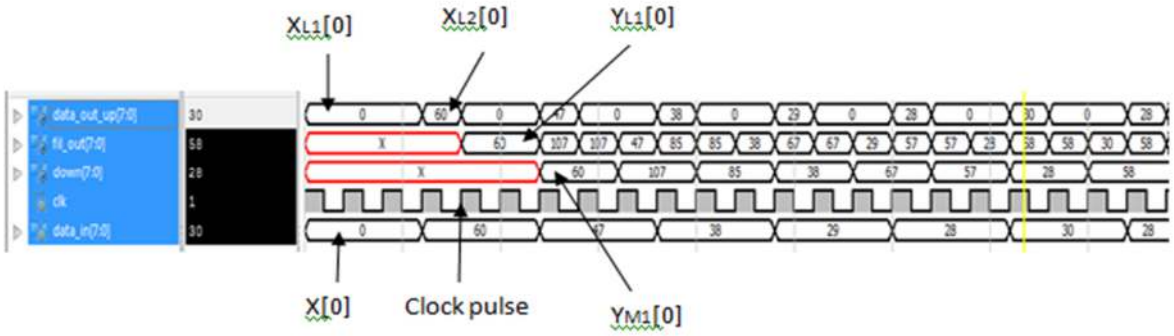


Figure 3.15: Timing Diagram of $L = 3$ and $M = 2$.

The timing diagrams of Figures 3.14 and 3.15 illustrate different cases. The Figure 3.14 shows the case I where we have used $L = 2$ and $M = 2$. In this case I we have mentioned the result parameters in Figure 3.14 that we have simulated in our proposed design operations. The data input as $x[n = 0]$ indicted as well as data upsampled by $L = 2$ between input data $x_{L(1)}(m = 0) = 0$ up-sampled data as $x_{L(2)}(m = 0) = 0$ within the single clock pulse. The filtered output data shows with respsect to input data $x_{L(1)}(m = 0) = 0$, the filtered output up-sampled data $y_{L(1)}(m = 0) = 107$ and for up-sampled data $x_{L(2)}(m = 0) = 60$ shows $y_{L(2)}(m = 0) = 107$ within the same single clock pulse. The final output shown after down-sampling operation by M=2 which shows as $y_m(m = 0) = 107$ after one clock pulse shift. Figure 3.15 shows timing diagram for case II $(L = 3, M = 2)$. Table 3.4 shows the timing summery of proposed Sampling Rate Conversion system for the case I.

Table 3.4: Timing Summary of Sampling Rate Conversion System.

Clock period	15.570 ns
Clock Frequency	64.226 MHz
Minimum input arrival time before clock	1.946 ns
Maximum output required time after clock	11.196 ns
Maximum combinational path delay	No path found

3.4.3 Result Analysis

Table 3.5 shows the first 10 EEG data and their corresponding outputs. Here up-sampled data are twice the input data for L=2 & M=2. Again, the up-sampled data is filtered by digital filter & finally we get the down-sampled data which is our desired output data. For simulation purposes, we have used 122 EEG data. The comparison of Input EEG data and Output EEG data is shown in figure 3.16. It is clear that data have been amplified by the filter for case I.

Table 3.5: First 10 data for L=2 & M=2 Case.

SL.	Data Input	Up Sampled Value	Filter Output	Down Sample/ output Data
01	0	0	107	107
		0	107	
02	60	60	145	85
		0	85	
03	47	47	114	67
		0	67	
04	38	38	95	57
		0	57	
05	29	29	87	58
		0	58	
06	28	28	86	58
		0	58	
07	30	30	88	58
		0	53	
08	28	28	94	66
		0	66	
09	30	30	117	87
		0	87	
10	36	36	180	104
		0	127	

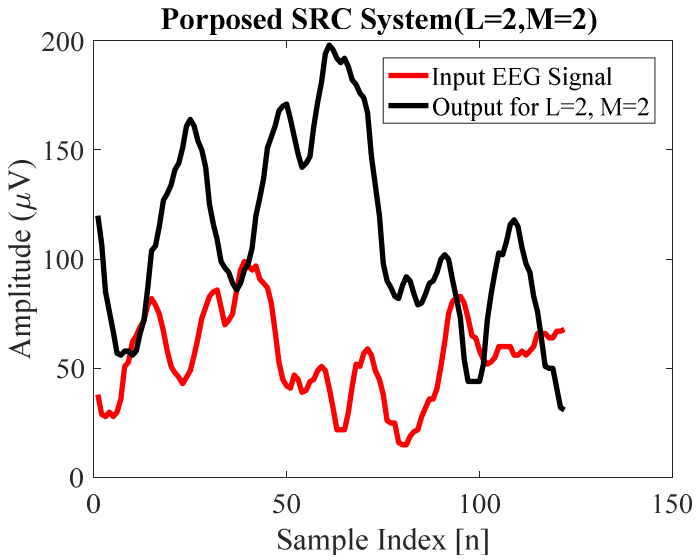


Figure 3.16: Result Comparison of Input and output EEG signals for $\boldsymbol{L = 2}$ & $\boldsymbol{M = 2}$.

Figure 3.16 illustrates a plot of the EEG data and its final output of Sampling Rate Conversion System. The results of case I has shown better results than case II. So, it is clear that higher up-sampling and down-sampling rate works better. Figure 3.16 and 3.17 the phase of the output signal is shifted as compared to the input signal due to delay. Case I and II have shown different way of SRC operations in proposed system design. Case II have shown sample values of EEG data increases than input EEG signal because of using the ratio L/M.

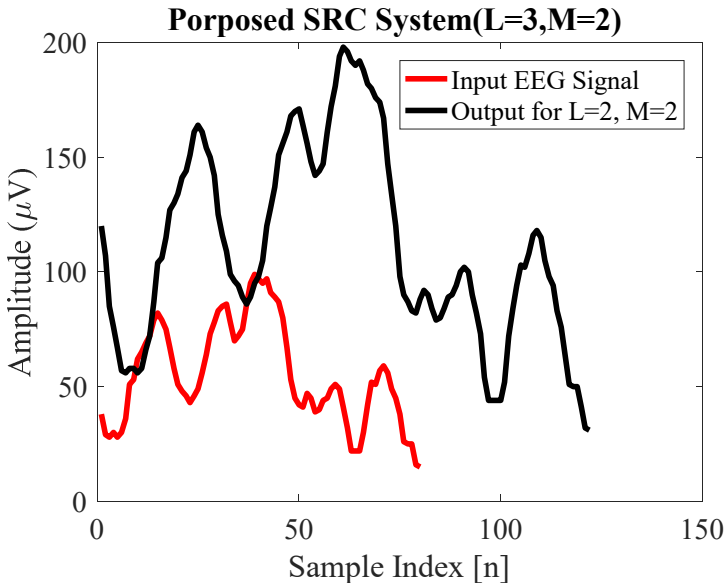


Figure 3.17: Result Comparison of Input and output EEG signals for $\boldsymbol{L = 3}$ & $\boldsymbol{M = 2}$.

Figure 3.18 shows a basic architecture for proposed design on SRC system using blocks of individual components for case I. The main components are coeffcients and data memories, analog input/output units (ADC and DAC), multiplier-accumulator (MAC), and a controller (not shown). The components of this proposed system can be implemented with fast, off-the-shelf products. Similar way we can develop for the case II in terms of change *L*.

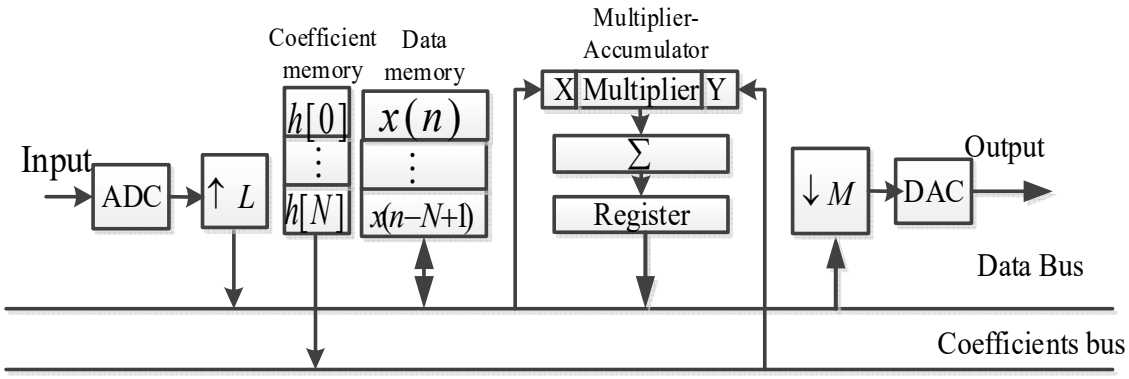


Figure 3.18: Architecture of sampling rate conversion system.

3.5 Summary

This chapter describes method I of design and implementation of sampling rate conversion system for EEG signal on FPGA Device. In this method I, the coefficient of the equation we have choosed is looked like a parabolic filter. The filter equation is a FIR filter. We haved considered two cases for justification of best multirate based approach of the proposed system. We have also checked different characteristics of a system like speeds, clock frequecnys, power consumpsions on HDL systhesis reports, power analysises, timing diagrams and figures using input signal and output signal. This proposed method I can be implementd on BCI system.

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CHAPTER IV

Sampling Rate Conversion System Method-II

Chapter Outlines

- Introduction
- Proposed Methodology II for Sampling Rate Conversion System
- Flowcharts of Sampling Rate Conversion System Method II
- Processing Algorithm of Sampling Rate Conversion System Method II
- Result Analysis and Discussion
- Summary
- References

CHAPTER IV

Sampling Rate Conversion System Method-II

4.1 Introduction

Sampling Rate Conversion system is the method of changing the sampling rate of a discrete signal to obtain a new discrete representation of the continuous signal. Due to noise and artifact into BCI system lost potential to improve accuracy. Proper filters need to be designed to filter these artifacts. Electrical activities of different body organ are described in [4.2]. The preprocessing chip design is done in this project based on FPGAs. Some researchers have done different methods for filter design as review, references [4.2-4.4], use Xilinx chips; [4.7-4.13] Altera devices; [4.1] both Xilinx and Altera; [4.4] both Orca and Xilinx; and [4.5] uses CLI. The system flow chart has been described in chapter 1. The data accuracy of this sampling rate conversion system is much higher than general filter methods.

4.2. Proposed Methodology II for Sampling Rate Conversion System

Proposed method consists of five module function (i) insert sample of EEG signal as an input, (ii) ADC, (iii) proposed digital filter, (iv) DAC, (v) finally output sample of EEG signal. The EEG signal was taken from the database, described in chapter 3. In signal processing system with a central digital engine, analog input and output signals, the analog input signal (usually after some amplification and filtering) enters into analog to digital converter (ADC) which converts it into a digital data stream. This stream is processed by the DSP core and the resulting digital output signal is reconverted into analog form by a digital-to-analog converter (DAC). DAC output is generally also proposed digital filter to obtain the analog output signal.

A simple block diagram representation of the proposed system using sampling rate conversion system where $h(n)$ is a proposed digital filter. The proposed filter have assigned some paprameters on input-output relationship for each block as in Figure 3.3 shown in chapter 3 and its signal flow

graph is shown in Figure 4.1. Each input sample fed in, three samples are computed. The non zero samples (that is the actual samples of $x(n)$ in the delay line are seperated by $L-1$ zeroes). Clearly , multiplication operations by the zero valued samples are unnecessary. Upsampled value is then fed into a complete filter. Output of filter data is down sampled by the sampling rate M. Down sampling M means to reduce sample according to the value of M. Here we have used $M=2$. This involves keeping the first sample discarding the next $M-1$ samples, keeping the next sample, and discarding the next $M-1$ samples, and so on.

Proposed filter equation of method are given below:-

$$y_1(n) = a_0 y_1(n-1) - b_0 x(n) \tag{4.1}$$

$$y_2(n) = c_0 y_2(n-1) - d_0 y_1(n) \tag{4.2}$$

The interpolation equation is

$$\mathrm{x}(n) = \mathrm{x}\left(\frac{n}{L}\right) \tag{4.3}$$

Now filter equation using up sampling as,

$$y_1\left(\frac{n}{L}\right) = a_0 y_1\left(\frac{n}{L}-1\right) - b_0 x\left(\frac{n}{L}\right)$$

$$y_2\left(\frac{n}{L}\right) = c_0 y_2\left(\frac{n}{L}-1\right) - d_0 y_1\left(\frac{n}{L}\right)$$

Decimation equation is,

$$x(n) = x(nM) \tag{4.4}$$

Filter output with down sampling equation is as follows:-

$$y_M(m) = \mathrm{y}_2\left(\frac{nM}{L}\right) \tag{4.5}$$

Where $x(n)$ represents the latest input sample, $x(n-1)$ the last sample, and $y_1(n)$ is the first step filter output data sequence, $y_2(n)$ is the final output data sequence of the filter and $y_1(n-1)$ and $y_2(n-1)$ are previous output. The parameters a_0, b_0, c_0 and d_0 are the filter coefficients. Coefficients $a_0 = 1$, $b_0 = 1$, $c_0 = 1$ and $d_0 = 1$. The simple digital filter structure is shown in Figure 4.1.

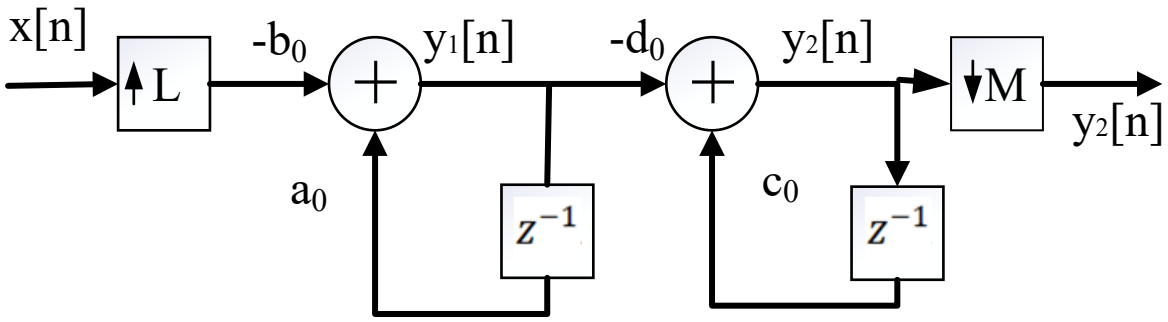

Figure 4.1: Proposed realization structure of a digital filter.

Equation for the digital filter is given below and applying z transform on the both side of the equation. Then rationalize the denominator, and the last step is to group it to real part and imaginary part. To compute the magnitude just use the Pythagoras theorem.

Applying z- transform at the both side of the equation (4.1), that means $x(n) = X(z)$, $y_1(n-1) = z^{-1}Y(z)$ *and* $y_1(n) = Y(z)$ and get,

$$Y(z) = z^{-1}Y(z) - X(z)$$

$$Y(z) - z^{-1}Y(z) = -X(z)$$

$$Y(z)(1 - z^{-1}) = -X(z)$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{-1}{(1 - z^{-1})} = -\frac{-z}{(z-1)} \tag{4.6}$$

Then substitute the z:

$$H(e^{j\omega}) = \frac{-e^{j\omega}}{(e^{j\omega} - 1)} \tag{4.7}$$

Expand to cos and sin:

$$H(e^{j\omega}) = -\frac{\cos(\omega) + j\sin(\omega)}{\cos(\omega) + j\sin(\omega) - 1} \tag{4.8}$$

Rationalize the denominator, group into real and imaginary part:

$$H(e^{j\omega}) = -\frac{\cos(\omega) + j\sin(\omega)}{\cos(\omega) + j\sin(\omega) - 1} \cdot \frac{\cos(\omega) - j\sin(\omega) - 1}{\cos(\omega) - j\sin(\omega) - 1}$$

$$= \frac{-e^{j\omega}.(e^{-j\omega} - 1)}{(e^{j\omega} - 1)(e^{-j\omega} - 1)}$$

$$= \frac{-e^{j\omega - j\omega} - e^{j\omega}}{e^{j\omega - j\omega} - e^{j\omega} - e^{-j\omega} + 1}$$

$$= \frac{-1 - \cos(\omega) - j\sin(\omega)}{2 - \cos(\omega) - j\sin(\omega) - \cos(\omega) + j\sin(\omega)}$$

$$= \frac{-1 - \cos(\omega) - j\sin(\omega)}{2 - 2\cos\omega}$$

$$= \frac{-1 - \cos(\omega)}{2(1 - \cos(\omega))} - j\frac{\sin(\omega)}{2(1 - \cos(\omega))} \quad (4.9)$$

Rearrange this equation and finally we get the magnitude response,

$$\left|H(e^{j\omega})\right| = \frac{\sqrt{(1 - \cos(\omega))^2 + sin^2(\omega)}}{2(1 - \cos(\omega))}$$

$$= \frac{\sqrt{1 - 2\cos(\omega) + cos^2(\omega) + sin^2(\omega)}}{2(1 - \cos(\omega))}$$

$$= \frac{\sqrt{1 - 2\cos(\omega) + 1}}{2(1 - \cos(\omega))}$$

$$= \frac{\sqrt{2 - 2\cos(\omega)}}{2(1 - \cos(\omega))} \quad (4.10)$$

Phase response of filter is as follows:-

$$\varphi(\omega) = \tan^{-1}\left(\frac{\frac{-\sin(\omega)}{2(1 - \cos(\omega))}}{\frac{-1 - \cos(\omega)}{2(1 - \cos(\omega))}}\right)$$

$$= \tan^{-1}\left(\frac{\sin(\omega)}{1 + \cos(\omega)}\right) \quad (4.11)$$

$H(z), X(n), Y(n)$ are described in chapter three details. $H\left(e^{j\omega}\right)$ is the Frequency response of the first equation of method II. $\left|H(e^{j\omega})\right|$ is the magnitude response of the first equation of method II and $\varphi(\omega)$ is the phase angle.

When $\omega = 0$, value of $\left|H(e^{jw})\right| = 0$ and $\left|H(e^{jw})\right| = 0.707 = 3dB$ when $\omega = 0.241\pi$

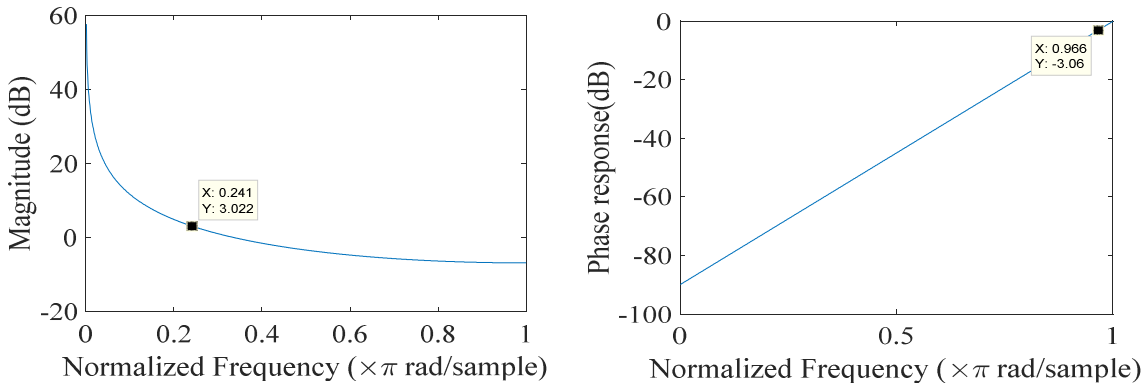

Figure 4.2: Frequency and Phase response of the first equation of method II.

So,

$$\omega = 0.241\pi$$

$$2\pi f = 0.241\pi$$

$f = 0.12$ Hz which is the digital frequency.

Analog cutoff frequency can drive from the value of digital frequency f

$$\frac{f_c}{f_s} = f$$

$$f_c = f f_s$$

Considering the sampling frequency is $f_s = 1000Hz$, then the cutoff frequency of frequency response would be,

$$f_c = 0.120 * 1000$$

$$= 120Hz$$

Let $z = e^{sT}$, where T=sampling period, since $s = \sigma + j\omega$, we have

$$z = e^{\sigma T} e^{j\omega T}$$

if $\sigma = 0$, then $|z| = 1$ and $z = e^{j\omega T} = \cos \omega T + j \sin \omega T$, i.e. the equation of a circle of unit radius in the z-plane. According to the figure of 4.3 The distance to the zero at z = 0 and the pole z = 1. This is a recursive IIR filter. For this filter in method II there is a single pole at z = 1. A filter will be stable when all the poles in the z-plane are within the circle that means z < 1. So, this filter unstable.

Apply z- transform at the both side of the equation (4.2),

$$Y(z) = z^{-1}Y(z) - Y(z) \tag{4.12}$$

Where right side $Y(z)$ of equation (4.12) is the output of the first equation (4.1). Applying z-transform to equation (4.1) we get, $Y(z) = z^{-1}Y(z) - X(z)$

So, the equation (4.12) can be rewritten as:

$$Y(z) = z^{-1}Y(z) - z^{-1}Y(z) + X(z)$$

$$Y(z) = X(z)$$

$$\frac{Y(z)}{X(z)} = H(z) = 1$$

Frequency response of the equation (4.2) is as follows:-

$$H\left(e^{jw}\right) = 1 \tag{4.13}$$

Magnitude Response would be:-

$$\left|H(e^{jw})\right| = 1 \tag{4.14}$$

Phase angle would be:-

$$\varphi(\omega) = \tan^{-1} 0 = 0$$

From Pole zero diagram of second equation of method II, it can say that the distance to the zero at z = 1 and the pole z = 1. The filter which is used in method II is a recursive IIR filter because input of the equation (4.2) depends on the output of the first equation (4.1). In this equation from the pole – zero diagram there is a single pole on the circle. As the value of pole z = 1, so that the filter is unstable (according to the condition of pole z is always less than 1).

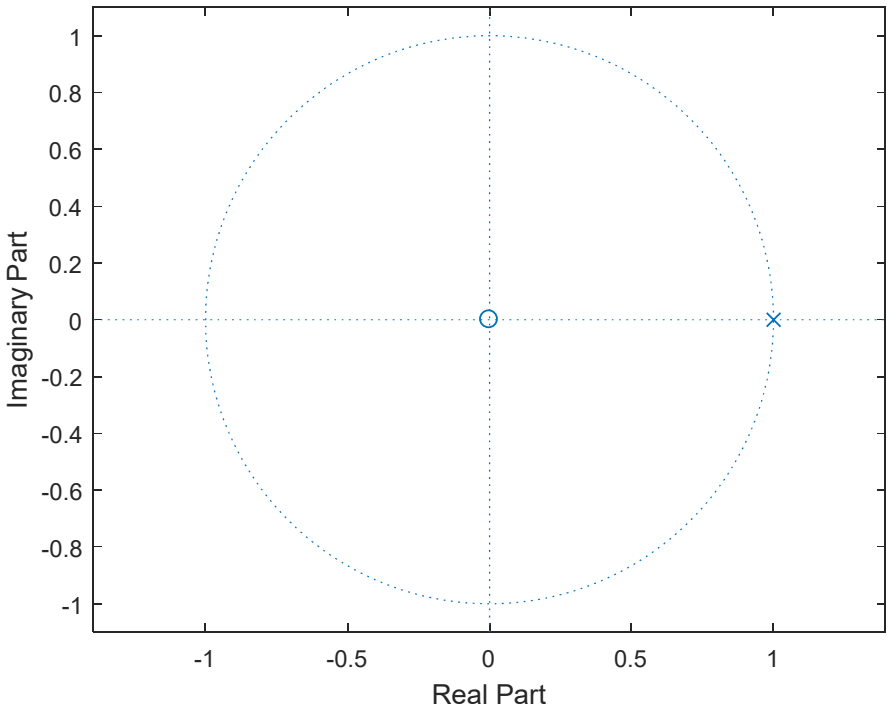

Figure 4.3: Pole-zero diagram of the first equation of method II.

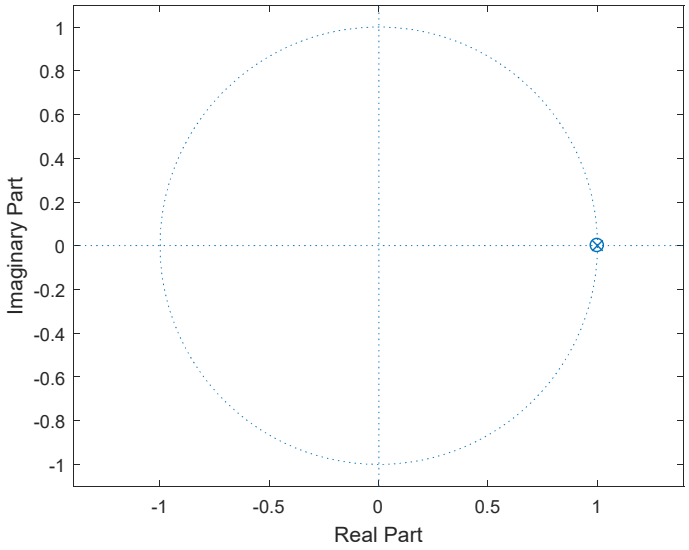

Figure 4.4: Pole-zero Diagram of the second equation of method II.

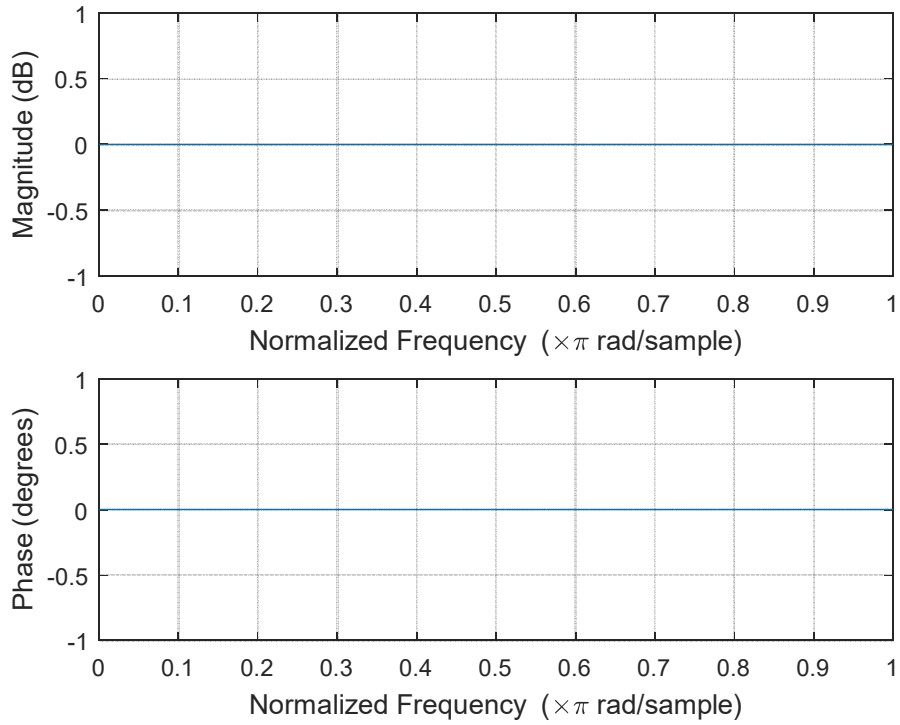

Figure 4.5: Frequency and Phase response of the second equation of method II.

4.3 Flowcharts of Sampling Rate Conversion System Method II

The proposed digital filter design is implemented based on the two equation (4.1) and (4.2). It is considered that, the coefficients of these equation are 8-bit quantized value. The main flow of work has done with N-point digital filter.

The proposed digital filter has at least four essential parts:

1) *Initialization:* Initialize system, this may include setting up a coefficient table.
2) *Input section:* this may include reading of the input sample, $x(n)$, e.g. from an ADC via a serial port.
3) *Inner loop computation:* The execution of the proposed system equation of the digital filter equation (4.1) & (4.2) to obtain $y(n)$.
4) *Output section:* This may include shifting/rounding of the result of the inner loop computation and sending this, e.g. to the DAC via a serial port.

As much of steps, 1, 2 and 4 are the system dependent; we will concentrate on the inner loop computation here. The proposed digital filter inner loop may be implemented with the following instruction in ALTRA Cyclone II board with processors EP2C35F672C6.

Figure 4.6 & 4.7 shows pipeline one element for configuration for arithmetic element for executing the equation (4.1) and (4.2). The arithmetic operations involved can be broken up into three distinct steps: memory read, multiply, and subtraction.

The coefficients, a_k, b_k, c_k and d_k and the data array are stored in memory as shown in Figure 4.6 & 4.7. In this case the coefficient and data memories are organized as shown in Figure 4.6 & 4.7. The auxiliary register AR1 is used for indirect addressing in the inner loop computation and initially points to the oldest data sample $y_1(n-1)$ and $y_2(n-1)$ in the data memory. The following procedure are executing in the inner loop such as

a. Adds the previous product to the accumulator- initially, the product is zero.
b. EEG signal decimal data are converted by ADC and stored x[n] data into auxiliary register AR1.
c. Increase the discrete samples data of x[n] by L (Interpolator) and stored L*x[n] data into register.
d. Multiply the coefficients b_k by the data memory $x(n)$ and store into AR1 and also a_k by $y_1(n-1)$ and store into AR2.-initially AR1 point's $x(n)$ and then successively, points $x(n-N+1)$ decrement the address by 1 and initially AR2 points $y_1(n-1)$ and successively, points $y_1(n-N)$ as it goes round the loop.
e. Subtracting the data AR1 from AR2 and store into AR3, which represent $y_1(n)$
f. Multiply the coefficient c_k by the data memory into AR4 and also d_k by the data memory into AR5. Initially AR4 points $y_2(n-1)$ and then successively points $y_2(n-N)$, similarly AR5 initially points $y_1(n)$ and successively points $y_1(n-N+1)$as it goes around the loop.
g. Subtracting the data from AR4 to AR5 and store into AR6, which represents $y_2(n)$
h. Decreasing the sampling rate of $y_2(n)$ by the factor of M and store it in register.
i. Final discrete output $y_2(n)$ and store into registor.
j. Apply $y_2(n)$ into DAC and get the values of $y_2(t)$.

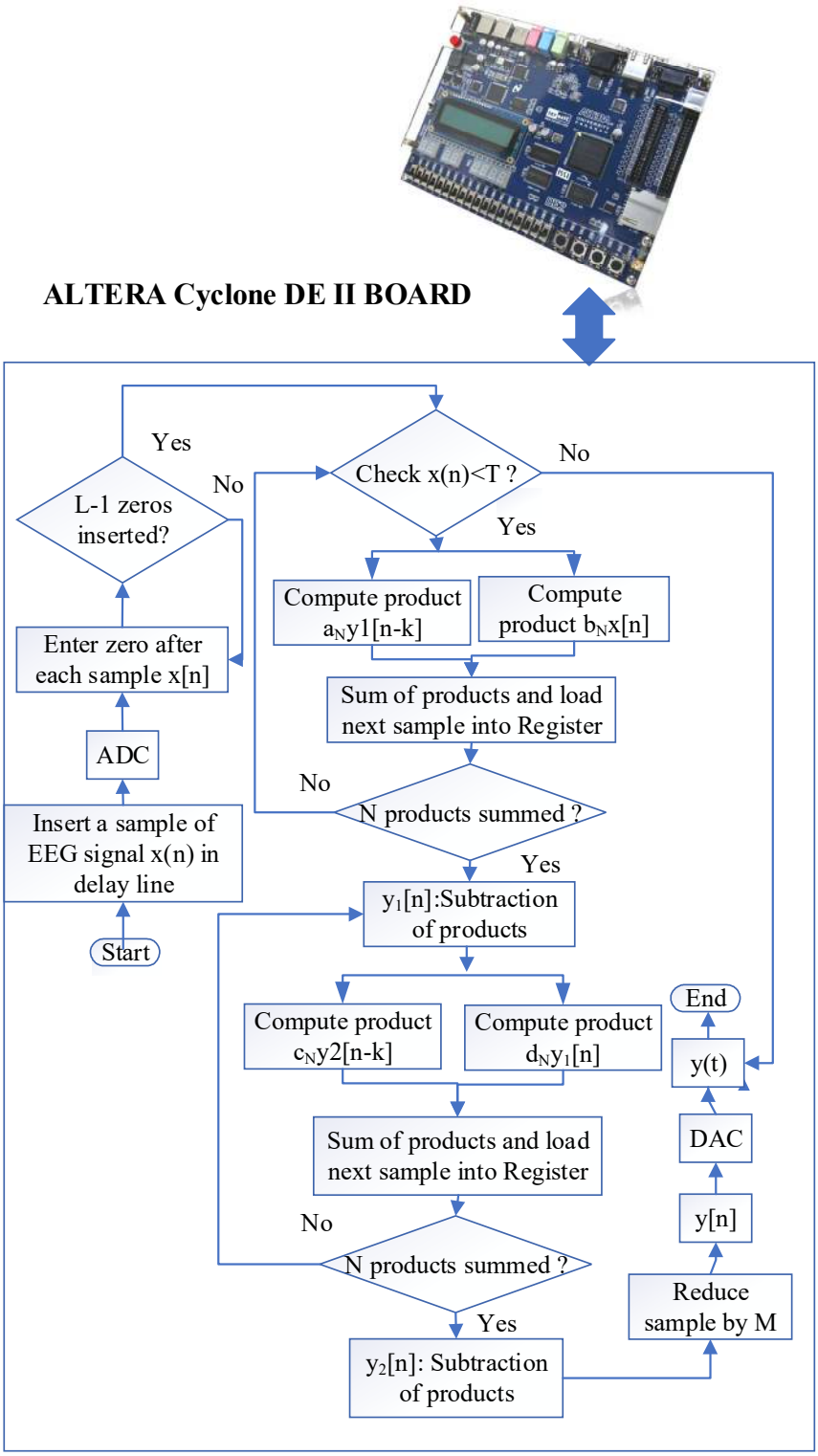

Figure 4.6: Flowchart of proposed SRC system methodology II.

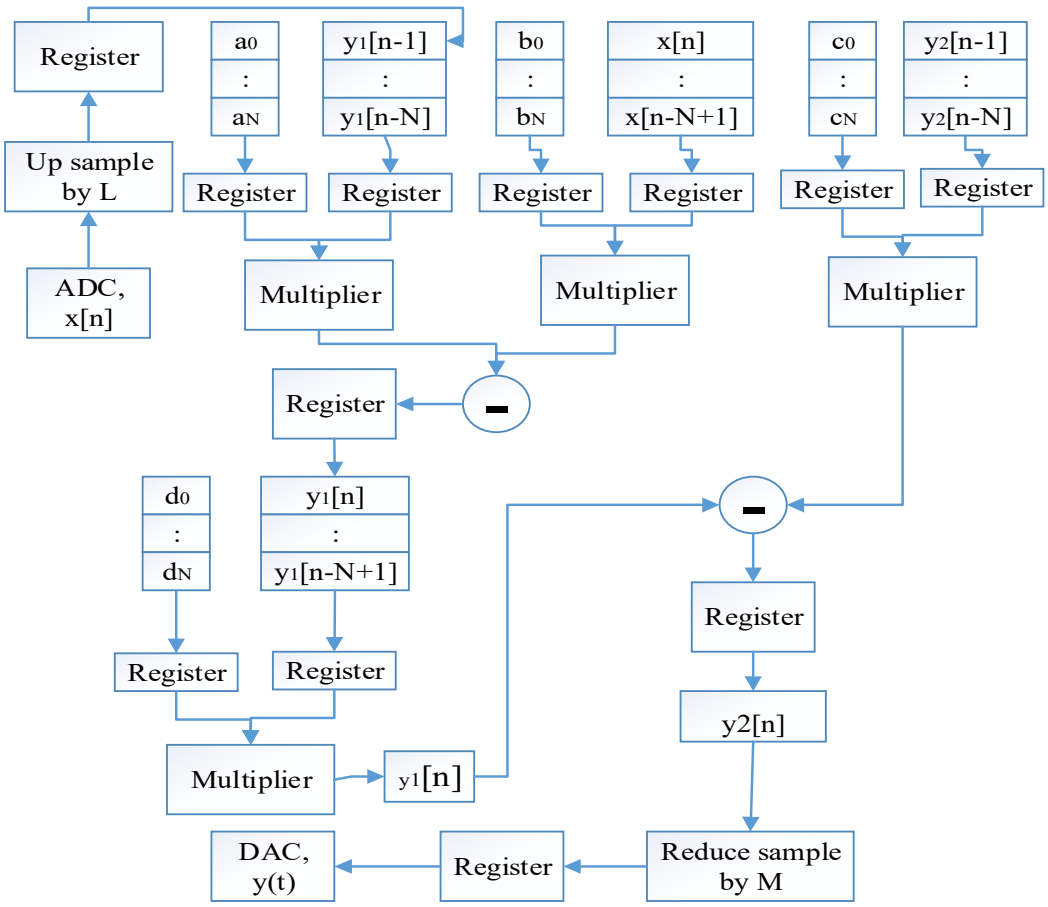

Figure 4.7: MAC of Proposed SRC System Method II.

4.4 Processing Algorithm of Sampling Rate Conversion System Method II

For real time novel digital filter of equations, the data and coefficients are stored in memory, conceptually, as shown in Figure 4.6 & 4.7. To appreciate how the proposed filter work of equation (4.1) & (4.2). Suppose the coefficients $a_0 = 1$, $b_0 = 1$, $c_0 = 1$ and $d_0 = 1$ of proposed filter which are given the following equations:

$$y_1(n) = a_0 y_1\left(\frac{nM}{L} - 1\right) - b_0 x\left(\frac{nM}{L}\right)$$

$$y_2(n) = c_0 y_2\left(\frac{nM}{L} - 1\right) - d_0 y_1(n)$$

These coefficients are fed from an ADC. The first things to do is to allocate two sets of contiguous memory locations (in RAM), one for storing input data $(x(n), x(n-1), y(n-1), y(n))$, and the other for the filter coefficients ($a_0 = 1$, $b_0 = 1$, $c_0 = 1$ and $d_0 = 1$) as depicted below:

Data in RAM	Coefficient Memory
0	$a_0 = 1$
0	$b_0 = 1$
0	$c_0 = 1$
0	$d_0 = 1$

At initialization, the RAM locations where the data samples are to be stored are set to zero since at the starting there is no data. The following operations are then performed.

Step 1: Read EEG data sample from EEG database from the ADC after threshold applied, shift data RAM one place (to make room for the new data), save the new input sample, compute output sample from Equation (4.1) and compute final output from Equation (4.2) and then send to the DAC: At initial stage, setting first positive clock pulse=1, reset=1, hold=0, and initial past sample output: $y(-1) = 0$.

Data in RAM	Coefficient Memory	Difference Equation
$x(0) = 0$	1	
$x(0) = 0$	1	
$y_1(0) = 0$	1	$y_1(0) = y_1(-1) - x(n) = 0$
$y(0) = 0$	1	$y_2(0) = y_2(n-1) - y_1(0) = 0$

Step. 2: Repeat the above operation at 2nd positive clock pulse=1, reset=0, hold=0 and workout the new output sample and send to the DAC:

Data in RAM	Coefficient Memory	Difference Equation
$x(0) = 0$	1	
$x(1) = 60$	1	
$y_1(1) = -60$	1	$y_1(1) = y_1(0) - x(1) = -60$
$y(1) = 60$	1	$y_2(1) = y_2(0) - y_1(1) = 60$

Step. 3: Repeat the above operation at 3rd positive clock pulse=1, reset=0, hold=0 and workout the new output sample and send to the DAC:

Data in RAM	Coefficient Memory	Difference Equation
$x(1) = 60$	1	

$x(2) = 47$	1	
$y_1(2) = 13$	1	$y_1(2) = y_1(1) - x(2) = 13$
$y(2) = 47$	1	$y_2(2) = y_2(1) - y_1(2) = 47$

Step. 4: Repeat the above operation at 4th positive clock pulse=1, reset=0, hold=0 and workout the new output sample and send to the DAC:

Data in RAM	Coefficient Memory	Difference Equation
$x(2) = 47$	1	
$x(3) = 38$	1	
$y_1(3) = 9$	1	$y_1(3) = y_1(2) - x(3) = 9$
$y(3) = 38$	1	$y_2(3) = y_2(2) - y_1(3) = 38$

Step. 8: Repeat the above operation at 8th positive clock pulse=1, reset=0, hold=1 and workout the new output sample and send to the DAC:

Data in RAM	Coefficient Memory	Difference Equation
$x(6) = 30$	1	
$x(7) = 28$	1	
$y_1(7) = 2$	1	$y_1(7) = y_1(6) - x(7) = 2$
$y(7) = 28$	1	$y_2(7) = y_2(6) - y_1(7) = 28$

Note that the oldest data sample has now fallen off the end.

Step. N: Repeat the above operation at nth positive clock pulse=1, reset=0, hold=0**,** past sample output: $y(n-1)$ and workout the new output sample and send to the DAC:

Data in RAM	Coefficient Memory	Difference Equation
$x(n-1) = N-1$	1	
$x(n) = N$	1	
$y_1(n) = \cdots$	1	$y_1(n) = y_1(n-1) - x(n) = \cdots$
$y(n) = \cdots$	1	$y_2(n) = y_2(n-1) - y_1(n) = \cdots$

Figure 4.7 shows a basic architecture for a novel digital filter using blocks of individual components. The main components are the coefficient and data memories, analog input/output

units (ADC and DAC), multiplier-accumulator (MAC), and a controller (not shown). The components of novel digital filter of equation (2) can be implemented with fast, off-the-shelf products.

At each sampling instant, a new data sample, $x(n)$, is read from the ADC and saved in the data memory. Each input data sample and the corresponding co-efficient are fetched from the memory simultaneously and applied to the multiplied. The products are then accumulated to yield the output sample. The computation of each output sample, $y(n)$, would require N-data-coefficient fetches from memory and N MACs.

4.5 Result Analysis and Discussion

Upsampling, Filtering and Downsampling operations are described in Chapter 3 For that reason, I don't described it here. RTL diagram, timing diagram and result analysis are described below.

4.5.1 RTL Diagram of Proposed System Method II

Register Transfer Level is a design abstraction which represents the flow of digital signal between hardware register and logical operations. RTL abstraction is used in Verilog and VHDL to create a higher-level representation of circuit from which lower level representation and actual wiring can be derived. RTL diagram consists of various segment. Each segment is described below.

Data input: The proposed system has given an input of 8-bit data.

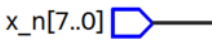

Figure 4.8: Input section of RTL Diagram method II.

Clk: It is used to generate clock pulses.

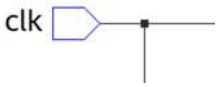

Figure 4.9: Clock section of RTL Diagram method II.

It is used to prevent any data to a threshold value above that it won't take that data and give the previous data.

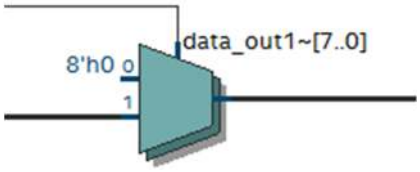

Figure 4.10: Threshold check of RTL Diagram method II.

It is d flipflop works on buffer [7:0] works enable for clock pulse.

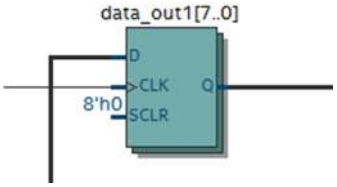

Figure 4.11: D Flip-Flop section of RTL Diagram method II.

It's the function of First step of digital filter, it will take the input value that stored in buffers x[n] and subtract from the previous output value of $y_1[n-1]$. The simple equation is:

$$y_1[n] = y_1[n-1] - x[n]$$

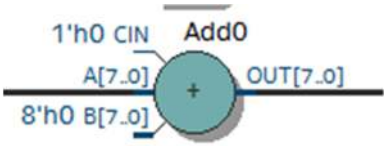

Figure 4.12: First Adder of RTL Diagram method II.

It's the second step of the digital filter, it will subtract the output of first step $y_1[n]$ from $y_2[n-1]$ The simple equation is:

$$y_2[n] = y_2[n-1] - y_1[n]$$

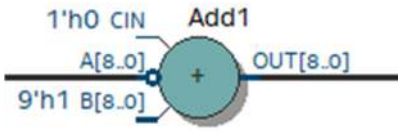

Figure 4.13: Second Adder of RTL Diagram method II.

It will give output data in 8 bit. If hold is used then $y_2[n] = y_2[n-1]$, if reset is used then $y_2[n] = 0$, if neither of that is used then $y_2[n] = x[n]$.

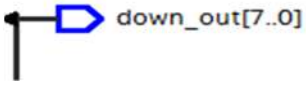

Figure 4.14: Output Section of RTL Diagram method II

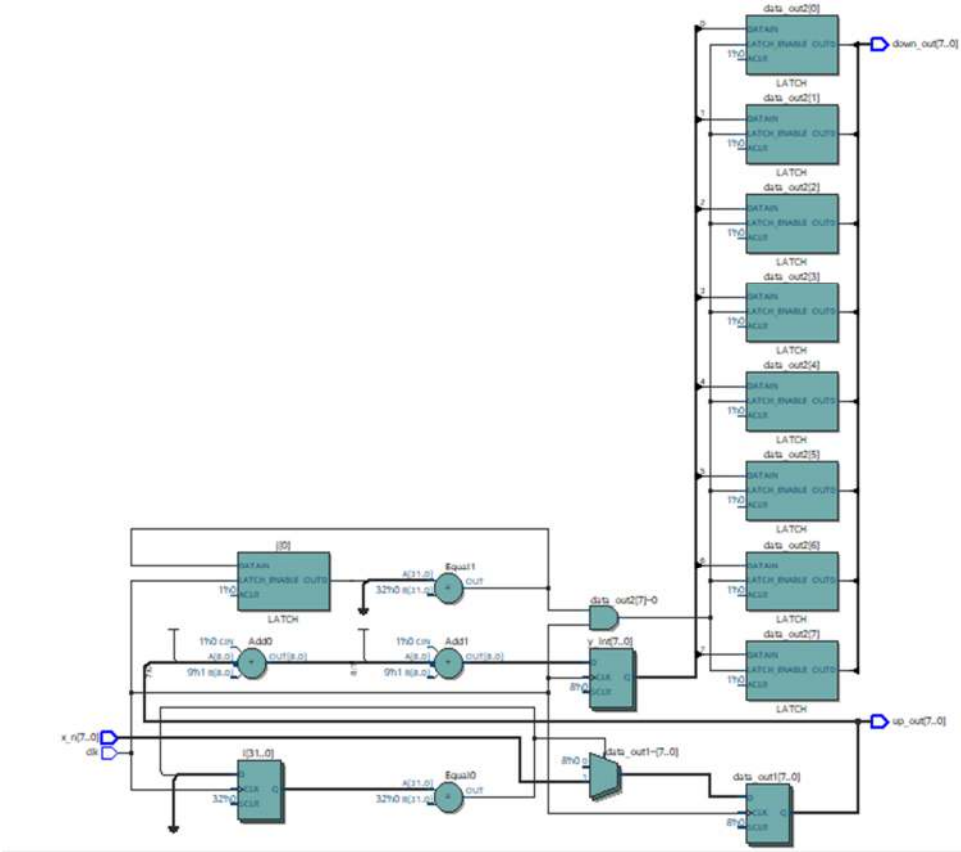

Figure 4.15: RTL Diagram of Proposed SRC System Method II.

In the total RTL block, multiplexers (MUX 2:1) and Lookup tables(4-LUT) have been used to generate logic operations. Here, registers have been used to store each and every data. Again,

multipliers, 8-bit adders, latches are used in the RTL diagram as shown in Table 4.1. Table 4.1 also shows the components of used in proposed system. Next, Table 4.3 shows that the core temperature was $27.1^{\circ}C$ during the simulation process. Table 4.3 also shows the voltage supply (V_{cc}), total current and total power needed for the proposed biochip design.

The figure 4.16 shows the timing diagram of input signal x[n] and the output signal y[n]. It will give output data in 8 bits. For the viewing comfort, all the input and output data are converted into decimal. 1st input sample is $x(n = 0)$. 1st output sample is $y[m = 0]$. clock pulse is also showed here. If hold is used then $y[n] = y[n-1]$, if reset is used then $y[n] = 0$, if neither of that is used then $y[n] = x[n]$.

Table 4.1 Resource utilization and latencies of arithmetic circuits

Estimated Total logic elements	Total register	Total logic elements	Logic element usage by number of LUT inputs		Dedicated logic register	Total I/O pins	Total Virtual pins	
6	9	6	4 input functions	2	9	25	0	
			3 input functions	15				
			2 input functions	10				

Table 4.2: Filter settings.

Options	Settings	Default value
Device	EP2C35F672C6	Device
Minimum Core Junction Temperature	0	
Maximum Core Junction Temperature	85	
Fit Attempts to Skip	0	0.0
Device I/O Standard	3.3-V LVTTL	
Use smart compilation	Off	Off
Enable parallel Assembler and TimeQuest Timing Analyzer during compilation	On	On
Enable compact report table	Off	Off

Auto Merge PLLs	On	On
Ignore PLL Mode When Merging PLLs	Off	Off
Router Timing Optimization Level	Normal	Normal
Placement Effort Multiplier	1.0	1.0
Router Effort Multiplier	1.0	1.0
Clock frequency	159.770MHz	

Table 4.3: Operating settings and condition.

Setting	Values
Nominal Core Voltage	1.20 V
Core temperature	27.1°C
Low Junction Temperature	0 °C
High Junction Temperature	85 °C

Table 4.4: Setup Time for Method II.

Data Port	Clock Port	Rise	Fall	Clock edge	Clock Reference
KEY[*]	KEY[0]	2.876	2.876	Rise	KEY[0]
KEY[1]	KEY[0]	2.876	2.876	Rise	KEY[0]
SW[*]	KEY[0]	0.986	0.986	Rise	KEY[0]
SW[0]	KEY[0]	0.445	0.445	Rise	KEY[0]
SW[1]	KEY[0]	0.381	0.381	Rise	KEY[0]
SW[2]	KEY[0]	0.226	0.226	Rise	KEY[0]
SW[3]	KEY[0]	0.312	0.312	Rise	KEY[0]
SW[4]	KEY[0]	0.140	0.140	Rise	KEY[0]

4.5.2 Timing Diagram of Method II

Timing diagram of Figure 4.16 shows for the equation (4.1) of method 2 and Figure 4.17 for the equation (4.2) of method 2. We can do results analysis for the equation (4.1) as in Figure 4.16, for the input value of $x(n=0)=0$ we get the output value of $y(n=0)=-60$, similarly for $x(n=1)=60$ we get the output value of $y(n=1)=-13$ and so on. When we used both equation (4.1) and (4.2) to get resulted the timing diagram shows Figure 4.17. For the input value of $x(n=0)=0$ we get the output value of $y(n=0)=60$, similarly for $x(n=1)=60$ we get

the output value of $y(n = 1) = 47$ and so on. The repsentation of red color sample shows in both timing diagram of Figure 4.16 and 4.17 denote the delay of the system.

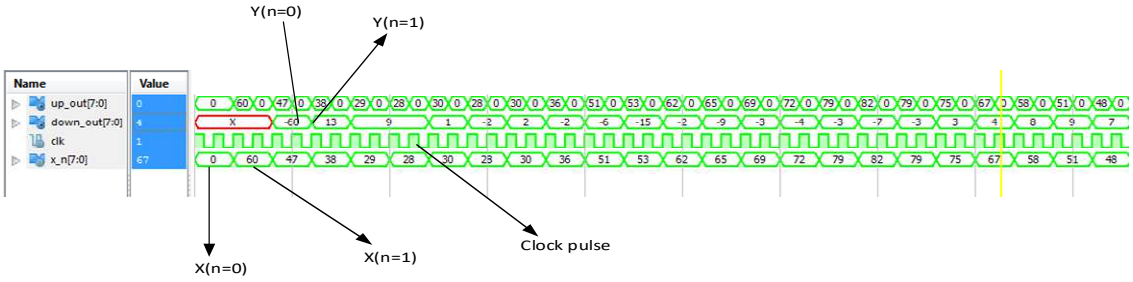

Figure 4.16: Timing diagram of proposed method 2 for 1st equation on EEG signal.

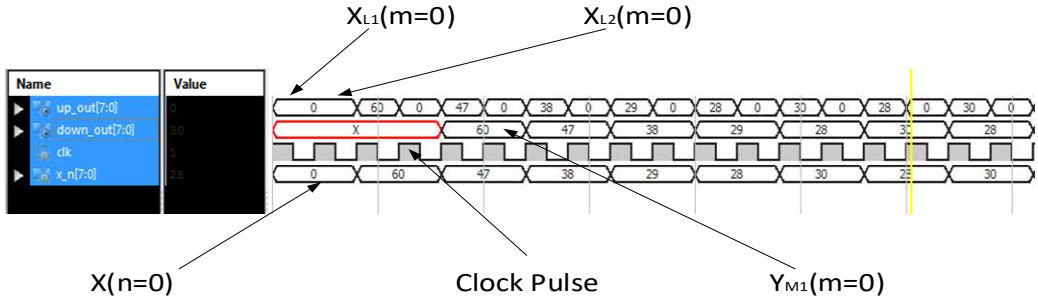

Figure 4.17: Timing diagram of proposed method 2 for 2nd equation on EEG signal.

4.5.3 Result Analysis

Following Table 4.5 shows the first 10 EEG data and their corresponding outputs. At first perform upsampling by $L = 2$ in the prospoed method II. Where the output of upsampled value is then pass through the proposed filter. After that process, the filter output is downsampled by $M = 2$. The sample value after downsample is the desired output of this system. In this method, most of the process shows same output as like as input sample value of EEG signal.

Figure 4.18 shows result of the second method of the Sampling Rate Conversion system. The display of red color is the input signal $x[n]$ and blue color is the output signal $y_2[n]$. There is finally same output as input signal. That is can be written by the equation $y_2[n] = x[n]$. From Figure 4.18 it is clear that the phase of the output signal is shifted as compared to the input signal. In the timing diagram 4.17 we can see that the output samples are shifted (presented by red color) due to delay. This result proves the robustness of good behavior chip for SRC system.

Table 4.5: Example of EEG data and corresponding output data

clk* 2	Reset	Hold	Input	1st eq Output(y1)	Output
0->1	1	0	0	0	0
0->1	0	0	60	-60	60
0->1	0	0	47	13	47
0->1	0	0	38	9	38
0->1	0	0	29	9	29
0->1	0	0	28	1	28
0->1	0	1	30	-2	30
0->1	0	0	28	2	28
0->1	0	0	30	-2	30
0->1	0	0	36	-6	36
0->1	0	0	51	-15	51
0->1	0	1	53	-2	53
0->1	0	0	62	-9	62
0->1	0	0	65	-3	65
0->1	0	0	69	-4	69
0->1	0	0	72	-3	72
0->1	0	1	79	-7	79
0->1	0	0	82	-3	82
0->1	0	0	79	3	79

Table 4.6: Multiplexer Restructuring Statistics (Restructuring Performance).

Multiplexer Inputs	4:1
Bus width	16bits
Baseline Area	32LEs
Area if restructured	16LEs
Saving if restructured	16LEs

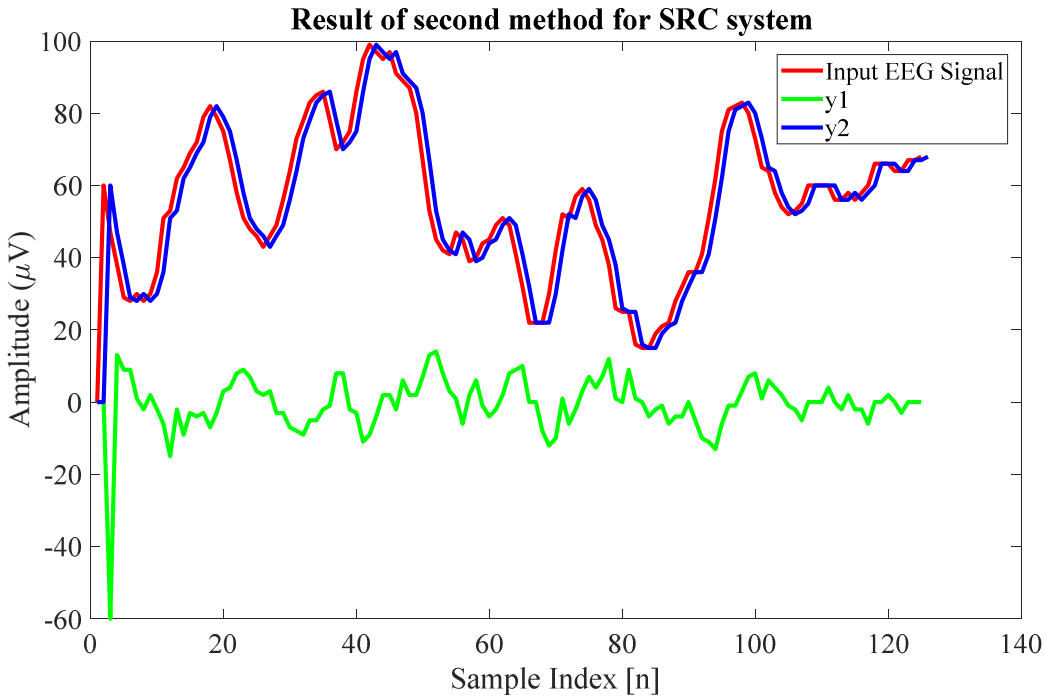

Figure 4.18: Final results for Sampling Rate Conversion system method II.

Figure 4.19 shows a basic architecture for proposed design method II on SRC system using blocks of individual components. The main components are coeffcients and data memories, analog input/output units (ADC and DAC), multiplier-accumulator (MAC), and a controller (not shown). The components of this proposed system can be implemented with fast, off-the-shelf products.

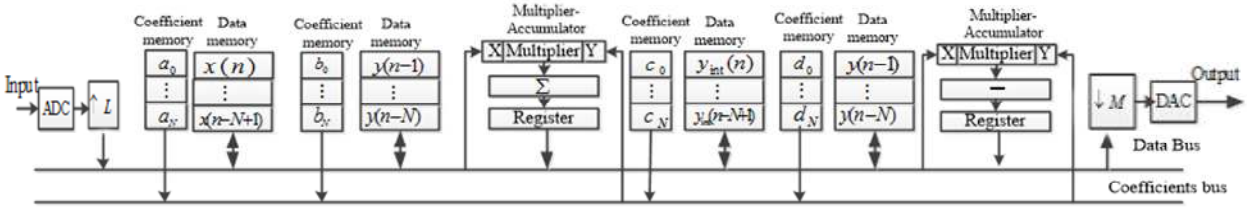

Figure 4.19: Architecture of SRC system method II.

4.6 Summary

This chapter describes method II of design and implementation a causal filter method II of sampling rate conversion system for EEG signal on FPGA Device. In this method II, we have

considered a LTI difference equation for recursive or causal IIR filter. Two equations have been considered to implement the recursive process. We have also checked different characteristics of system like speed, clock frequecny, power consumpsion on HDL systhesis report, power analysis and timing diagram and plotted figure using input and output EEG signal. This proposed method II is implementd as preprocessing chip for BCI system.

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CHAPTER V

Conclusion and Future Work

Chapter Outlines

- Conclusion
- Future Work

CHAPTER V

Conclusion and Future Work

5.1 Conclusion:

We have presented an easy and simple approach design and implementation sampling rate conversion for EEG signal on FPGA Device. In this system, considered two methods where the SRC method 1 has been used two cases for justification of best multirate based approach of the proposed system. Also, SRC based digital filter with differential equation is developed in second method for noncausal system. System characteristics such as performance parameters: speed, clock frequecny, power consumpsion on HDL systhesis report, power analysis and timing diagram are also checked. In the future, this model can be enhanced and developed with larger dataset to apply into BCI system. So, it will be interesting to know how medical techonolgy uses this proposed method in patient monitoring system for simple and fast diagonosis.

5.2 Future Work:

In the future, proposed Sampling Rate Conversion System model and proposed chip can be enhanced and developed with larger dataset to apply into Brain Computer Interface (BCI) system, Medical science for research, patient monitoring system and athlete body monitoring system etc.